

Overview of Design Methodologies

Lecture 1

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Hardware Description Languages (HDLs)

- Highly portable
- Describe multiple levels of abstraction
- Provide many descriptive styles
 - Structural
 - Register Transfer Level (RTL)
 - Behavioral
- Serve as input to synthesis
- Support structured design methodology

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HDL-based Design Flow

- Create behavior
- Consider testability
- Verify/simulate functionality
- Synthesize gate-level Netlist
- Compare gate-level and behavior
- Conduct fault analysis
- Verify timing
- Place & route
- Verify design rules
- Extract parasitics

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Design Styles

- ASIC
 - examples: controllers
 - typical characteristics
 - low cost
 - slower speed
 - specific applications
 - short development time
 - older manufacturing technologies
 - mass market
 - ASIC designs can be large in size
 - millions of transistors and more

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Processor Designs

- Designs that follow architectural SPECs
 - microprocessors, signal processors, etc.
 - Typical characteristics
 - architectural specification
 - long development time
 - expensive
 - fixed market
 - high performance
 - state-of-the-art manufacture facilities

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Memory Designs

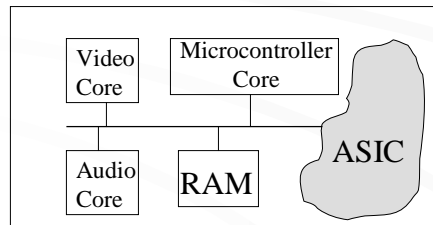
- On-chip / off-chip storage devices
 - video RAM, flash memory, etc.
 - high density
 - high performance
 - regular structure
 - special design methodology
 - special manufacture facilities
 - growing market
- Memory designs are crucial in many high-performance applications

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Embedded Design

- Core-based design or IP design
- Current hot market
- New challenges in tools/methodologies
- Heterogeneous system-on-a-chip

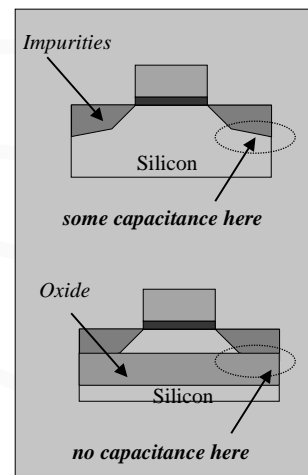


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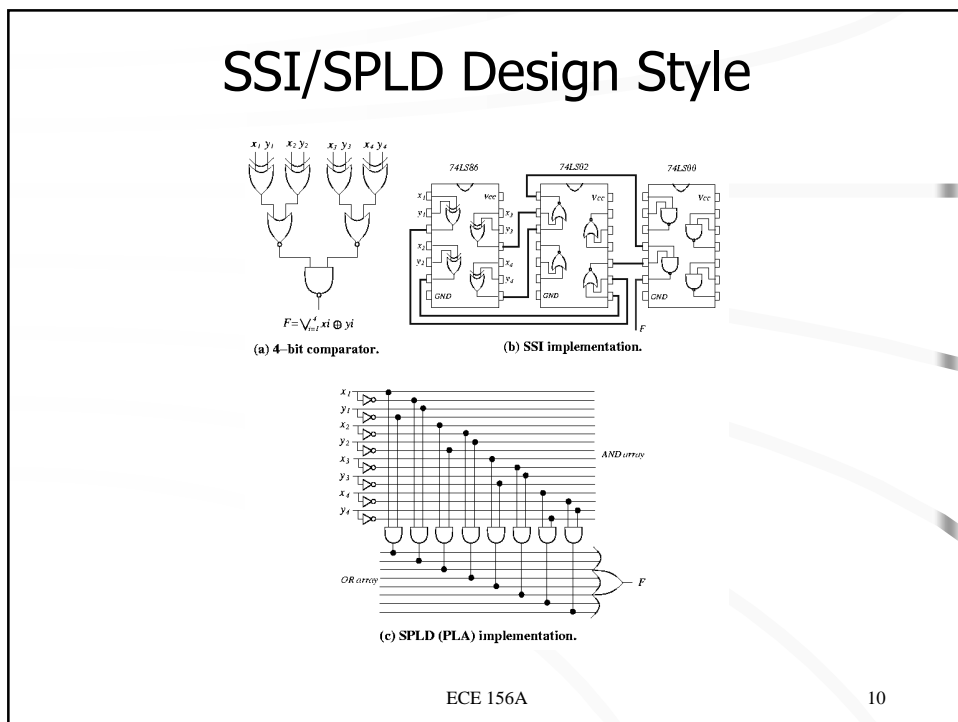
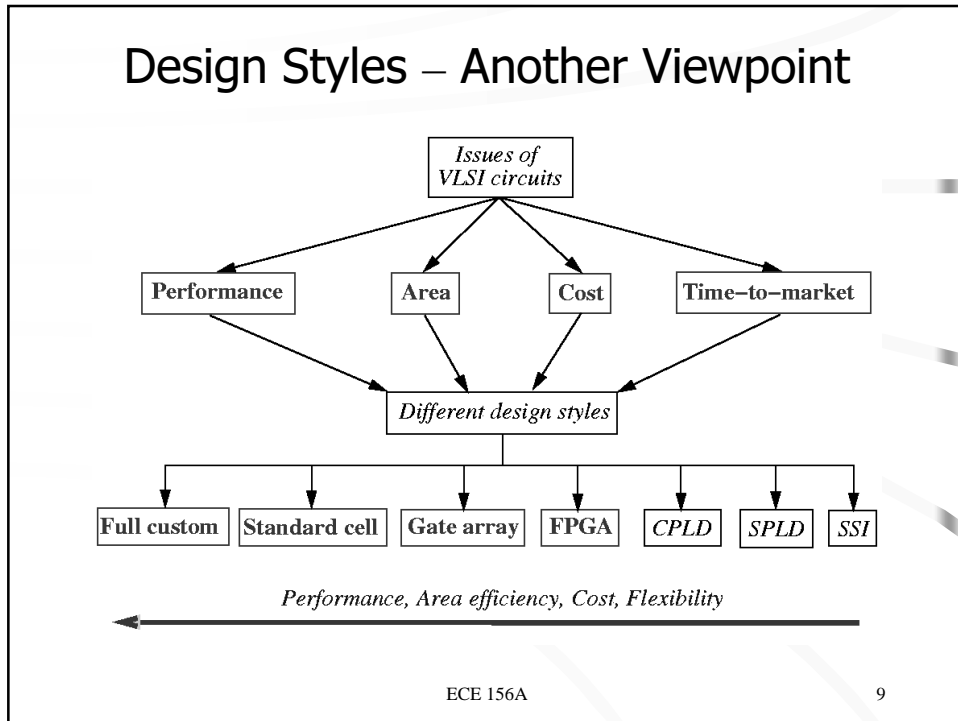
Today's Designs

- Tens of millions of transistors
- 2-4 GHz
- Deep sub-micron (≤ 0.13)
- Complex manufacture process
 - Copper wiring
 - Silicon-On-Insulator (SOI)
 - Many Metal Layers
- Mixed-signal applications



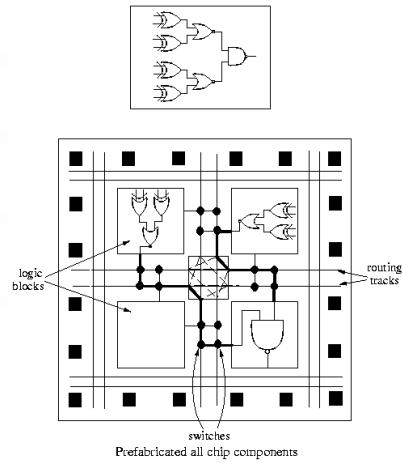
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FPGA Design Style

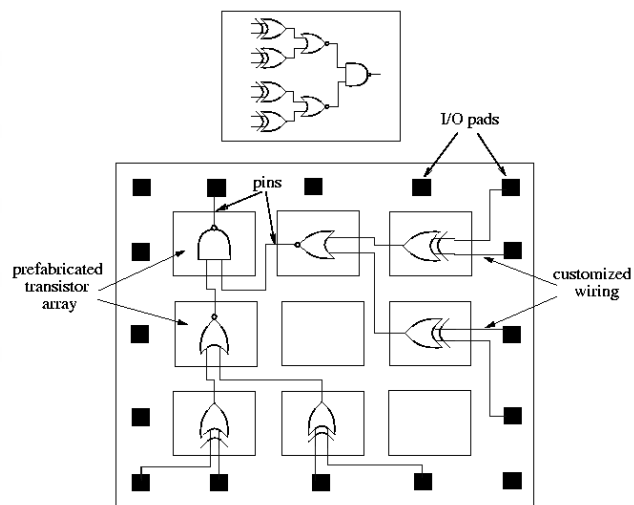
- Illustrated by a symmetric array-based FPGA:



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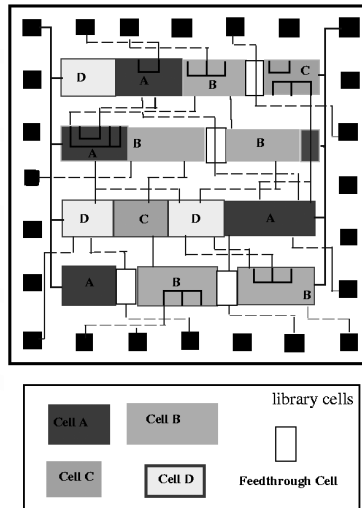
Gate Array Design Style



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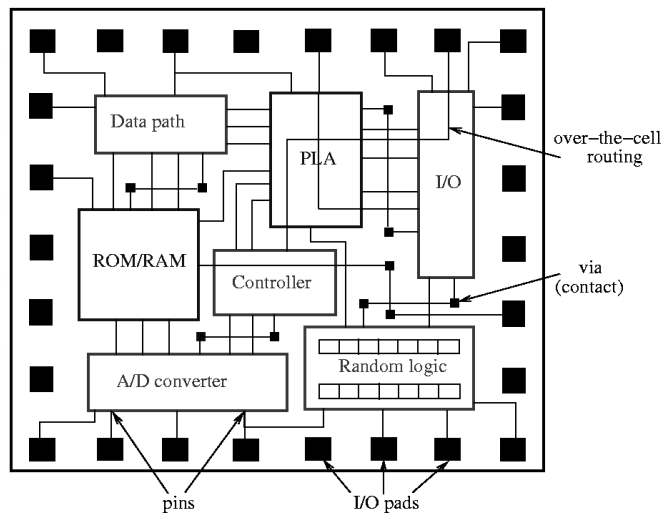
Standard Cell Design Style



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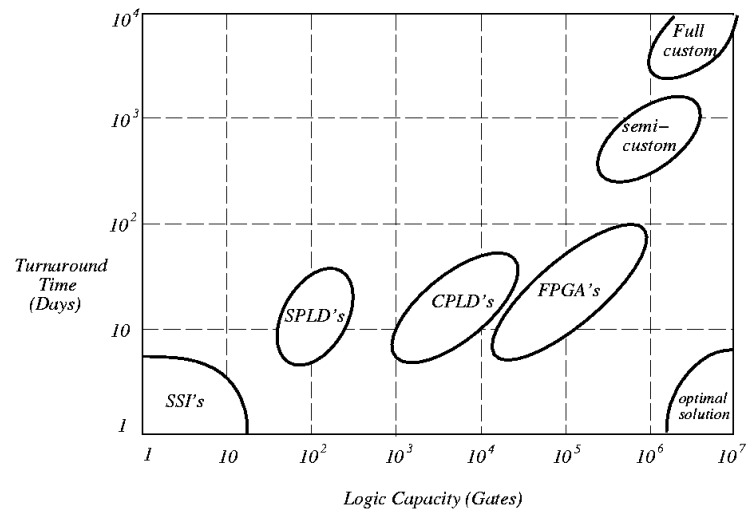
Full Custom Design Style



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Design Style Trade-offs



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Design Styles

- Restricting design styles to reduce complexity.
- Choosing design style according to design time, performance, size and cost, etc.

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Typical Design Flow - Industry

- Obtain product requirements
- Derive design specification
- Construct simulation model
 - Behavior and/or RTL
- Perform functional verification
- Synthesize to gate level model
- Logic minimization/ Design for Test
- Place and route/ Physical analysis
- Tapeout

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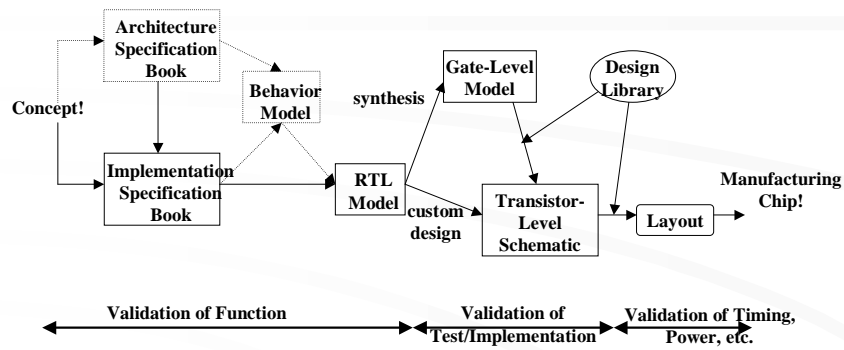
Post Design - Industry

- Setup manufacture line
- Obtain first silicon
- Diagnosis of defects/ Yield improvement
- System bring-up test
- Silicon debugging/ On-chip repair
- Mass production/ Speed grading
- Ship to customers

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Design Flow Overview



- Post-silicon debug time is increasing and may exceed the pre-silicon design time

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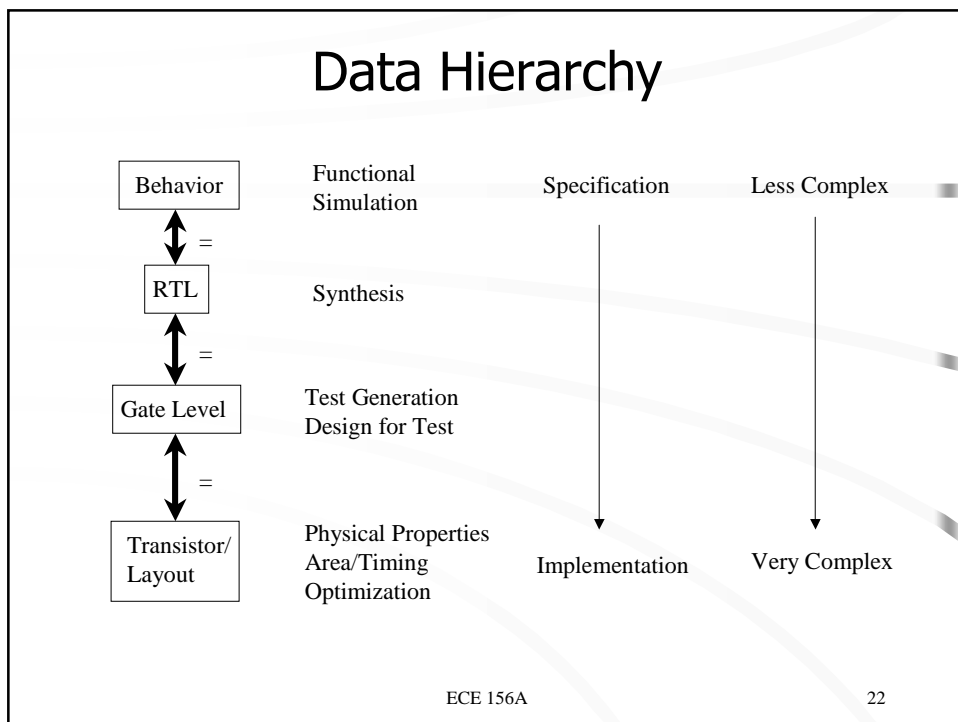
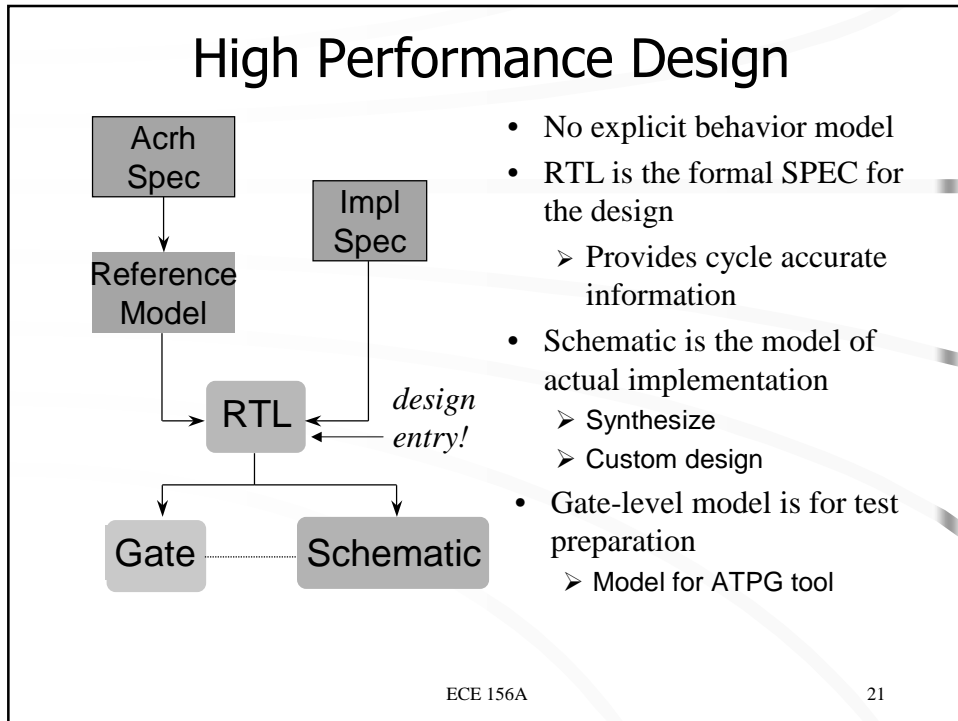
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Design Data Hierarchy

- Behavior
 - Like a C program
- RTL (Register Transfer Level)
 - *Explicitly define all state-holding elements*
 - *Provide a cycle-accurate model*
- Gate
 - All high-level constructs (if, case, assign) are converted to gates (and, or, not).
- Transistor
 - All are converted with nmos, pmos, etc.
- Layout (final picture)

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Challenges

- **Functional Verification**
 - What functions do we need?
 - How do we know the design performs all functions we want?
- **Equivalence Checking**
 - Specification = Implementation?
- **Test Preparation**
 - A chip is manufactured correctly?
- **Performance Constraints**
 - Timing, power, noise are ok?

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In Practice

- **No behavior model**
 - time-to-market pressure
 - can be useless next time
 - has to implicitly exist in a simulator
- **No gate-level model**
 - old design (in schematics) re-use
- **Tools are broken - always**
- **Too many formats to handle**
 - Every tool and every person have their own views to do things

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Quality Issues

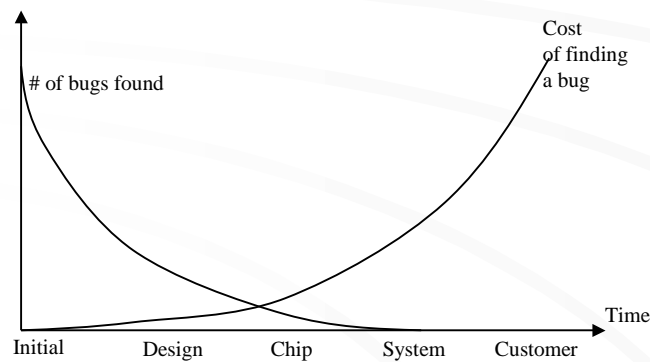
- How do we know we have done a good job?
 - Never can be sure?
 - Can our customers find out?
 - How is your manager going to say to his/her manager?
- How do we know what it is going wrong?
 - Locate a design error or manufacturing defect
 - Analysis the cause
 - Go back and fix the design or the process
 - can be costly

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Do Everything Early

- Because the later you have a problem, the higher price it will cost you



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No Perfect Solution

- Validation is done by a collection of approaches - no magic solution
 - Check it many times
 - Check from different perspectives (angles)
 - Use different tools
 - Use different people
 - designer <> verification engineer
 - We only say that it is ok after we exhaust all means we can think of

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Jobs

- Designs
 - Architecture Designer
 - Logic Designer
 - Circuit Designer
 - Verification Engineer
 - DFT Engineer
- Tools
 - Methodologist
 - Tool Developer
 - Application Engineer

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Design Companies

- Microprocessors
 - Intel, SUN, Motorola, TI, IBM, AMD, etc.
- Signal Processors
 - TI, Lucent, Intel, etc.
- Memory
 - SamSung, Micron, etc.
- Embedded Cores
 - ARM, Motorola, Intel, TI, IBM, MIPS, etc.

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EDA Tools Companies

The diagram illustrates the EDA tool flow across different design levels. On the left, a vertical stack of boxes represents the design stages: Behavior, RTL, Gate Level, and Transistor/Layout. Each stage is connected to the next by a double-headed arrow with an equals sign (=). On the right, various EDA tools and companies are mapped to these stages:

- Behavior:** Functional Simulation (Synopsys)
- RTL:** Synthesis (Synopsys)
- Gate Level:** Test Generation, Design for Test (Mentor Graphic)
- Transistor/Layout:** Physical Properties, Area/Timing, Optimization (Cadence); schematics (Cadence); Place & route (Advanti! (Synopsys))

Company affiliations are shown with arrows: Synopsys and Mentor Graphic are linked to IBM; Cadence is linked to Berkeley; Advanti! is linked to Synopsys.

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This Course

- Design behavior code
- Design RTL code
- Learn about validation, verification, and test
- Build the basis for
 - A career in the semiconductor industry
 - A career in the EDA industry

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Information

- TA Office Hour
 - 1-2pm, Mon. and 2-3pm, Wed.
- Remember to register your software online in order to use Verilog features
 - For Xilinx student edition
- Homework:
 - Study online help; play with the software
 - Get online Verilog Tutorial

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Using Design Compiler

- At the beginning, you can use any Verilog simulator to check the correctness of your Verilog code
- Later in the quarter, I will introduce you the synthesis tool, Synposys Design Compiler (DC)
 - There will be a few exercises using DC
 - You will need an account at the ECI lab
 - Please open an account at the ECI lab if you haven't had one
 - I will give a tutorial on DC in one of the W 4-7 labs (to be announced later)