Process Design Kit and Design Automation for Flexible Hybrid Electronics

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Abstract—High-performance low-cost flexible hybrid electronics (FHE) are desirable for internet of things (IoT). Carbon-nanotube (CNT) thin-film transistor (TFT) is a promising candidate for high-performance FHE because of its high carrier mobility (25cm²/V.s), superior mechanical flexibility/stretchability, and material compatibility with low-cost printing and solution processes. Flexible sensors and peripheral CNT-TFT circuits, such as decoders, drivers and sense amplifiers, can be printed and integrated with thinned (<50μm) silicon chips on soft, thin, and flexible substrates for appealing product designs and form factors. Here we report: 1) process design kit (PDK) to enable FHE design automation, from device modeling to physical verification, and 2) open-source and solution-process proven intellectual property (IP) blocks, including Pseudo-CMOS [1] digital logic and analog amplifiers on flexible substrates, as shown in Figure 1. The proposed FHE-PDK and circuit design IP are fully compatible with silicon design EDA tools, and can be readily used for co-design with both CNT-TFT circuits and silicon chips.

Index Terms—Flexible hybrid electronics, thin-film transistors, carbon-nanotube, thinned silicon chips

I. INTRODUCTION

Flexible and printable TFTs have exponential growth in performance and cost reduction in recent years, which enables new applications such as disposable sensors, RFID tags, and low-cost internet of things (IoT) [2], [3]. To design a large-scale (>1,000 transistor count) TFT circuitry that is manufacturable with low-cost printing or solution processes, however, is another story. Due to large printing process variations as well as the lack of complementary and reliable TFTs, large-scale TFT circuits often suffer from higher power consumption and low circuit yields, particularly in low supply voltages. These limitations make TFT circuits targeting IoT or wearable applications a significant challenge.

On the other hand, the hybrid-integration of thinned silicon chips and printable TFTs on the same flexible substrate emerges as a viable solution. The printable sensors and TFT circuits that benefit from low manufacturing cost and conformal form factors can be an ideal complement to rigid silicon chips for designing a flexible IoT or wearable device. We have previously reported our progress of developing FHE-PDK and simple circuits with CNT-TFTs [4], [5]. We imagine that an ideal FHE-PDK should include: 1) simulation models of printable passive and active devices, such as TFTs, resistors, inductors, and capacitors, 2) design rules of printable devices given the limitations of specific printing or solution process capability, 3) multi-physics simulation models that can capture the interaction among electrical-thermal-mechanical performance, and 4) co-design capability with silicon chips, ideally using the same design environment or EDA tools.

Based on these requirements, in this paper, we report the following progress regarding FHE-PDK: i) simulation models of printable passive and active devices, such as TFTs, resistors, inductors, and capacitors, 2) design rules of printable devices given the limitations of specific printing or solution process capability, 3) multi-physics simulation models that can capture the interaction among electrical-thermal-mechanical performance, and 4) co-design capability with silicon chips, ideally using the same design environment or EDA tools.

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Fig. 1: Open-source circuit design IP, including Pseudo-CMOS [1] digital logic, analog amplifiers, and passive elements. (Left) solution-processed circuit design IP blocks on a 10μm flexible substrate for bending test, and (right) design IP blocks on a 1μm flexible substrate.

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To investigate the effective mobility of fabricated TFTs, we observed that the effective mobility $\mu_{eff}$ is enhanced as the $|V_{GS}|$ increases for both CNT-TFT and IGZO-TFT, when $|V_{GS}|$ is relative small [8]. Similar mobility dependency phenomenon has been observed in OTFT and a-Si TFT [6], and the commonly accepted theories are based on charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [6]. This common phenomenon among different TFT technologies encourages us to build a unified model to capture fundamental behaviors of different TFTs based on TDTs and VRH assumptions.

1) Mobility Enhancement: Both theories indicate the field enhancement of the mobility:

$$
\mu = \begin{cases} 
\mu_0(V_G - V_{th})^\gamma, & \text{N-type TFT} \\
\mu_0(V_{th} - V_G)^\gamma, & \text{P-type TFT} 
\end{cases}
$$

(1)

, where $V_{th}$ is the threshold voltage, $\gamma$ is the field enhancement factor for mobility and $\mu_0$ is defined as the effective mobility when $|V_G - V_{th}| = 1$. This mobility enhancement assumption explains the increase of the effective mobility at a low $|V_{GS}|$.

2) Contact Effect: The degeneration of mobility at high $|V_{GS}|$ can be explained partially by the contact resistance $R_S$ and $R_D$ at source/drain terminals. These resistances result in effective gate-source/drain-source voltage drops: $V_{DS} = V_G - R_SI_{DS}$, $V_{DS} = V_D - (R_S + R_D)I_{DS} = V_D - R_CI_{DS}$, where $R_C = R_S + R_D$ and the current with contact effect is denoted as $I_{DS}$. The derivations are not presented here for simplicity and the contact effect can be illustrated as follows:

$$
I_{DS} \approx \frac{WC_{ox}\mu}{L[V_G - V_{th}] - \frac{1}{2}V_{DS}}I_{DS}
$$

(2)

$$
\frac{I_{DS}}{I_{DS}'} = \frac{\tilde{\mu}}{\mu} = \frac{1}{1 + kR_C(V_G - V_{th})}; \quad k = \frac{W}{L}C_{ox}\mu
$$

(3)

We can conclude that contact resistances lead to mobility reduction with a factor of $1/(1 + kR_C(V_G - V_{th}))$ and it becomes more significant as $|V_{GS}|$ increases, which explains the degeneration of the effective mobility with a high $|V_{GS}|$. CNT-TFT has relative larger $k$ comparing to IGZO-TFT $k_{CNT} \approx 25k_{IGZO}$, thus leading to more obvious mobility degeneration [8].

3) Surface Roughness Effect: As gate voltage increases, electrons tend to flow closer the channel surface. Due to the low-cost fabrication process of TFTs, interface traps and surface roughness lead to degeneration of the effective mobility [9]:

$$
\frac{\tilde{\mu}}{\mu} = \frac{1}{1 + \theta(V_G - V_{th})};
$$

(4)

Here, $\theta \propto 1/t_{ox}$ is a parameter related to the thickness of the gate oxide. This phenomenon combining with the contact effect leads to an overall mobility drop with a factor of $1/(1 + (\theta + kR_C)(V_G - V_{th}))$. Although, surface roughness and contact effect have identical formula with a term $V_G - V_{th}$, their physical explanations are different. The experimentally-extracted model parameters for CNT, IGZO, and organic TFTs are shown in Table II. More details regarding the unified TFT model can be found in [8].
Field effect mobility extracted based on an idealized MOS-FET current model has been widely used for TFT performance benchmarking. With the field-dependent properties, the extracted mobility could vary significantly at different effective gate voltages. Therefore, to better evaluate the TFT performance, the combination of the low field effect mobility ($\mu_0$) and the field-dependent factor ($\gamma$) should be used. In this way, the unified compact model can enable accurate SPICE simulations for TFT technology and design benchmarking [8].

### B. Resistor Models

In addition to TFTs, the CNT film can also be used to realize a linear resistor and the manufacturing process of a CNT resistor is fully compatible with CNT-TFTs. The CNT resistors have a wide range of applications such as linear and transimpedance amplifiers. Figure 4 shows the conceptual representation of a CNT resistor structure. The resistance is determined by the width $r_1$ and the length $r_2$. $R = \rho * r_2 / r_1$, where $R$ is the resistance and $\rho$ is the sheet resistance $\approx 135K \Omega$. To further study the CNT resistor linearity and process variations, we fabricated and characterized 864 CNT resistors on a flexible substrate shown in Figure 2. With 40 $\mu$m resistor width, the length is varied from 2 $\mu$m to 100 $\mu$m and the measurement results are shown in Figure 4. We can learn that the CNT resistors show a good linearity when the length is greater than 10 $\mu$m, when compared against a linear fitting curve. Figure 5 further reveals the process variations of the CNT resistors, where 96 test samples are included for each case of the resistor lengths 10 $\mu$m, 50 $\mu$m, and 100 $\mu$m, and 384 samples are included for the case of the length 20 $\mu$m. While the histograms follow Gaussian distributions, we can learn that the standard variations $\sigma$ reduces when the resistor length increases. For the resistor modeling, as shown in Fig. 6, the parasitic capacitance and inductance are not included for simplicity. The resistor model contains both the intrinsic resistance as well as the contact resistance between the CNT film and the contact metal. Thus the total resistance $R_{total}$ includes the contact resistance $R_c = R_{cs} + R_{cd}$ for two terminals and the channel resistance $R_{ch}$. Here, $R_{ch}$ is the sheet resistance of the channel.

$$R_{total} = R_c W + R_{ch} L W$$  \hspace{1cm} (5)$$

From Eq. (5), we can see that the $R_{total}$ is a linear function versus the resistor length $L$ while keeping the resistor width $W$ as a constant. The $R_c / W = 11.6 K \Omega$ is the intersection when $L = 0$ and $R_{ch} / W = 2.46 K \Omega$ is the slope of the linear fitting curve, as illustrated in Fig. 6.

### C. Capacitor Models

In addition to CNT resistors, flexible capacitors can also be realized using CNT-TFT compatible solution process for
Fig. 6: Measured CNT resistor characteristics against various resistor lengths of 10µm, 20µm, 50µm, and 100µm. The channel width is 40µm.

Fig. 7: Conceptual representation of a parallel-plate capacitor using the width (c1) of the top-plate metal to define the capacitance.

applications such as ac-coupled amplifiers or low-pass filters. We use simple parallel-plate top and bottom metals to realize the flexible capacitors as shown in Figure 7, where the width c1 of the top metal is used to define the capacitance and the Al2O3 dielectrics thickness is 25nm. To further study the process variations of the capacitance, we designed and characterized 431 parallel-plate capacitors as shown in Figure 2 and the measurement results can be found in Figure 8 for the capacitor width c1 from 45µm to 1415µm. We can learn that while the standard variations σ of the unit capacitance (fF/µm²) are similar for different capacitor widths, the average unit capacitance decreases with a larger width. We suppose that this phenomenon is due to thinner dielectrics for larger-sized capacitors. The 2D spatial analysis in Figure 9 shows the unit capacitance variations across the same flexible substrate, with which figure we can learn that the unit capacitance is higher at the center of the substrate. This could be attributed to the thinner dielectrics at the center. An equivalent model of a parallel-plate capacitor can be found in Figure 10. The experimentally-extracted values of the series resistance $R_s$ is around 1.5Ω and the parallel resistance $R_p$ is around 1MΩ. The intrinsic capacitance can be defined as $C_{\text{intrinsic}} = C_{\text{unit}} \times W^2$, where $C_{\text{unit}}$ is the unit capacitance around 3 fF/µm² and W represents the capacitance width.

III. PHYSICAL DESIGN VERIFICATION

To enhance the productivity of FHE circuit design, we incorporate mainstream EDA tools for FHE-PDK design verification and create experimentally-proven design rules of CNT-TFTs, CNT resistors, and parallel-plate capacitors, inductors etc using printing or solution processes. Based on these design rules, we create technology files using Standard Verification Rule Format (SVRF), T-cl or Python based formats to perform
Fig. 10: Equivalent model of a parallel-pate capacitor. $R_s$ is the series resistance due to thin electrode (40nm thick) and through-layer VIAs. The $R_p$ is the parallel resistance due to $Al_2O_3$ dielectrics.

Fig. 11: The physical design verification flow (ex. DRC) for a CNT resistor based on experimentally-derived design rules.

Fig. 12: Different types of parasitic capacitors and resistors

Physical verification with mainstream EDA tools such as Mentor Graphics Calibre. The physical design verification flow (ex. DRC) is illustrated in Figure 11. In addition to physical design verification, we also incorporate material properties to create technology files for layout-parasitics extraction (LPE). Layout-related parasitics in flexible circuits can be significant compared with silicon chips, which is due to larger physical footprints. Thus, it is essential to include accurate estimates of layout-related parasitics for post-layout simulations, particularly for high-performance FHE circuits. As shown in Fig. 12, the parasitic capacitance including intrinsic and fringe capacitance can be derived using the mainstream LPE tools with the knowledge of material properties such as dielectric constants and dielectric thickness etc, as well as the physical design information. Parasitic resistors are mainly attributed to metal layers as well as the layer-to-layer VIAs. After the parasitics extraction and back-annotation to the circuit netlist, post-layout simulations can be performed to include the layout-dependent parasitics for flexible circuits.

IV. OPEN-SOURCE CIRCUIT DESIGN IP

A. Digital Logic

To overcome the design challenges such as the lack of complementary reliable TFTs as well as large process variations for printed and solution-processed TFT circuits, we have previously reported a robust design style Pseudo-CMOS [1]. Based on Pseudo-CMOS, we have developed a variety of solution-process proven digital logic circuit IP blocks ranging from a simple inverter, NAND gate (Figure 13), ring oscillators (Figure 14), to shifter registers using CNT-TFT compact models [8].
CNT-TFTs within a short period of time. The simulated CNT-TFT circuit performance and power-consumption also provide a good correlation with the fabricated CNT-TFT circuits. The open-source digital circuit IP blocks are experimentally-proven to be operable at low supply voltages (3V). This benefit can ease the FHE power circuit design for supplying both CNT-TFT circuits and silicon chips on the same substrate.

B. Analog Blocks

In addition to digital TFT logic circuits, we have also developed key analog building blocks for FHE-PDK users, such as a 9T-1C tunable-gain amplifier as shown in Figure 15. The voltage gain can be tuned by varying the gate-bias voltages VTUNE of the feedback CNT-TFT. The physical size of the 9T-1C amplifier is only 350x350 μm². The input capacitor is used to attenuate low-frequency input noises and block the dc feedback to the input terminal. The measured waveforms can be found in Figure 16 with 32.7 dB gain at 33.2 KHz. The input capacitor can also be replaced with a CNT resistor for signal amplification on low-frequency inputs.

V. CONCLUSION

In this paper, we report our progress in developing a PDK for FHE design and verification. While FHE is emerging as a viable solution for high-performance low-cost IoT and wearable applications, the device models, design rules, and technology files are still missing to enable the co-design and co-simulations of flexible TFT circuits and thinned silicon chips. FHE-PDK fills these gaps by providing open-source device models, design rules, technology files, and circuit design IP blocks. We also benefit from using FHE-PDK to design a variety of digital and analog circuit IP blocks with a good confidence of the fabrication results, using printing or solution processes. We believe that the proposed FHE-PDK will be the must-have toolbox for FHE designers.

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