Vertical Integration of Memristors onto Foundry CMOS Dies using Wafer-Scale Integration

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Abstract

As Moore's law scaling approaches its physical limit, there is increased interest in memristors as a replacement to transistors in memory applications due to their smaller footprint and superior scaling characteristics. However, memristors are intrinsically two-terminal devices, requiring an underlying CMOS control interface for proper operation. Thus the integration of CMOS and memristors is essential to the development of memristor technology. Accordingly, hybrid configurations have been proposed that make use of the advantages of CMOS while utilizing a high density of memristors. However, memristor/CMOS hybrid fabrication is not trivial because high-density memories require memristor dimensions to be much smaller than those of the underlying CMOS. Additionally, memristors typically make use of materials not allowed in conventional CMOS fabrication. These issues point to a post-CMOS fabrication approach. An associated consideration for memristor/CMOS hybrid fabrication is the high cost of whole wafer fabrication. While whole wafer fabrication of memristors is viable for large volume markets, it is not a practical route for niche applications or research. While this suggests the use of CMOS dies, edge effects typically set the minimum processable die size, as in the case of edge beads, which limit the achievable resolution of devices. To address these issues, we present a hybrid integration approach for post-CMOS vertical integration of memristors that is independent of CMOS die size. Our approach enables the vertical integration of memristors with small foundry-fabricated dies using a wafer-scale integration scheme. We demonstrate this approach using a 2.2-mm × 3.2-mm CMOS die fabricated in a standard dual-poly, three-metal 0.5-µm technology process. We use solution-processed BCB as an adhesive to embed CMOS dies into silicon wafer handles, allowing for easy handling and compatibility with a variety of lithography techniques such as electron-beam, nanoimprint and photolithography. The process is compatible with spin-coated planarization layers, such as polyimide or BCB, if nanometer-scale roughness is desired. As a demonstration, vertically integrated Ag/SiO_2/Pt switches were fabricated on CMOS using conventional photolithography techniques in a university cleanroom and tested through the CMOS circuitry. The measurements were compared to those of Ag/SiO_2/Pt switches fabricated off-chip in a similar process and indicate that the memristor/CMOS hybrids were fully functional. We believe this hybrid approach will pave the way for hybrid CMOS-memristor chips, enabling applications from neuromorphic computing to high-density memories.

Introduction

The continued drive for higher memory density integration coupled with the looming limit of CMOS scaling has increased interest in memristors as a replacement to transistors for memory applications [1], [2]. A memristor is a two-terminal device with a resistance that depends on the history of applied voltage [3], [4]. Memristors scale well down to the nanometer scale, to date functioning with active areas as small as 8 nm × 8 nm [5]. In addition to their use as memory, memristors' analog functionality allows them to serve as an artificial synapse for neuromorphic computation [6], [7], [8], [9]. To make use of the advantages of CMOS while utilizing a high density of memristors, hybrid memristor/CMOS approaches such as CMOL have been proposed that use a single CMOS selector transistor to address many memristors [6], [10].

The fabrication of such memristor/CMOS hybrids is not straightforward because memristor dimensions are ideally much smaller than that of the underlying CMOS. Additionally, the vast majority of memristor materials are not available as part of a standard foundry process. Accordingly, several groups to date have integrated memristors with CMOS on whole wafers or with modifications to the standard foundry process [11], [12], [13], [14], [15], [16], [17], [18]. Because such approaches may be prohibitively expensive without special access to a foundry, it is preferable to use standard foundry CMOS dies and fabricate memristors by post-processing. Recently, Lin et al. [19] successfully demonstrated a post-processing scheme for 3D integration onto a CMOS die using nanoimprint lithography, but their process is costly, using a die larger than 600 mm^2 for a device area of 0.25 mm^2. Such large die sizes are used to mitigate edge effects, e.g. from edge beads arising from spin coating, and also to accommodate the use of processes typically optimized for larger samples, such as chemical mechanical polishing.

Our approach employs wafer-scale integration [20], [21], [22] of millimeter-scale CMOS dies, which significantly reduces the cost of the CMOS and allows for post-processing of memristors using a variety of technologies and architectures. We use solution-processed BCB as an adhesive and planarization layer to embed CMOS dies into large silicon wafer handles, which allows for easy handling and renders edge effects inconsequential. This approach also allows for the use of solution processed planarization layers such as polyimide or BCB if nanometer-scale roughness is required. As a demonstration, we fabricated Ag/SiO_2/Pt resistive switches onto a CMOS die and recorded measurements through the CMOS circuitry.

Chip Design and Fabrication

CMOS design: The CMOS chip was designed as a memory controller to select, program and read the integrated memristors. A double decoding scheme [23] was used to select 8 bits of memory that could be programmed in parallel and read out serially. The layout of the chip is shown in Fig. 1.

The double decoding scheme was used in anticipation of implementing a CMOL crossbar architecture in the near future. The CMOL concept is illustrated in Fig. 2 [24]. In order to decouple the CMOS feature size from that of the crossbars, the crossbars are rotated relative to the underlying CMOS. Active memristor areas are formed at the intersections of the crossbars. The red and blue pins represent the interface between the underlying CMOS and the crossbars. Each red and blue pair forms a CMOS cell, which comprises of transmission gates and drive circuitry that supply the appropriate voltages to the electrodes. For any given red pin, there are multiple nearby blue pins that can be addressed to select a unique memristor in a crossbar.

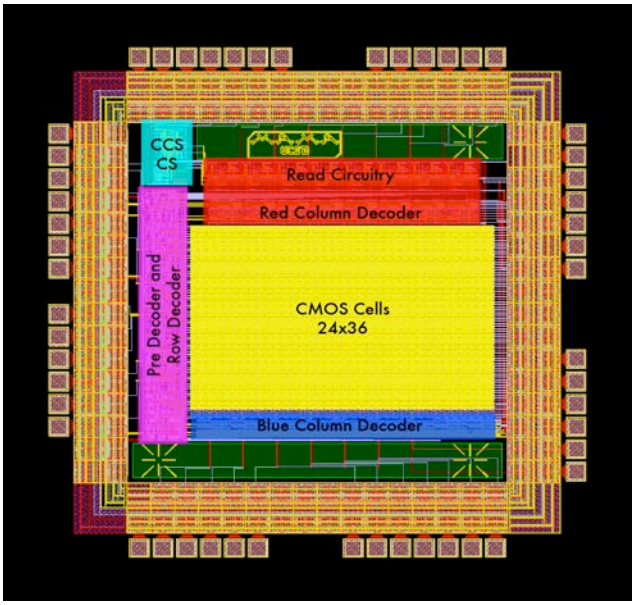

Figure 1. Chip layout.

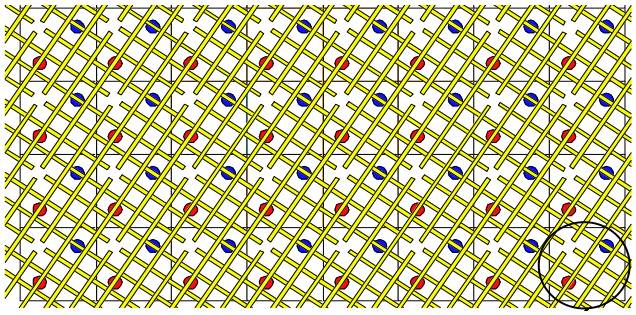

Figure 2. CMOL concept. The circle highlights the CMOS cell, as explained in the text. In this example each red pin is connected to twelve unique memristors. Figure is taken from [24].

Detailed information on the CMOS design is available in Payvand et al. [25]. The 2.2-mm × 3.2-mm CMOS die was ordered through MOSIS and fabricated in a standard dual-poly, three-metal 0.5-µm ON Semiconductor process.

Die embedding process: We have previously reported [26] a method for integrating CMOS dies onto silicon carrier wafers, which was adapted for this effort. CMOS dies as received had an approximately 1.7-µm silicon oxynitride passivation layer and Al pads in metal 3 for contacting memristors as top layers. Two 100-mm Si wafers were used for the integration process: a sacrificial wafer and a handle. First, a die-sized cavity was formed in the handle using the die as an exposure mask and using SiO_2 as an etch mask for a through-wafer Bosch deep RIE etch as reported in Uddin et al. [20]. The handle and the CMOS die were then bonded to the sacrificial wafer using Cyclotene 4024-40 BCB [27], [28] in a process to be reported elsewhere. The sacrificial wafer was removed with an SF_6/Ar RIE etch and the BCB was removed with an O_2/CF_4 ash.

Contact to Al pads: To access the Al pads in metal 3, windows were patterned through the silicon oxynitride with a CHF_3 ICP-RIE etch. AZ300T photoresist stripper was used at 80 °C to remove an insulating aluminum oxyfluoride layer which results from fluorine-containing dry etches that stop on Al [29]. To protect the pads after removing the oxyfluoride layer, the device pads and wire bonding pads were patterned using AZ P4110 and AZ400K 1:4 developer and a Au/Pt layer was deposited by electron beam evaporation and lifted off. All subsequent metal patterning followed the same process. An optional BCB planarization step could have been performed at this point, with windows etched through the BCB to make contact to the device and bonding pads.

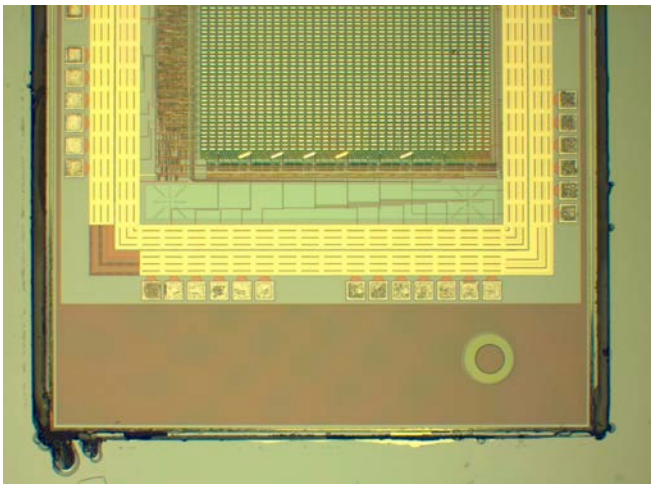

Figure 3. CMOS die integrated in handle after BCB ashing and protection of pads with Au/Pt.

Fabrication of memristors: After patterning the Au/Pt layer, Ag/SiO_2/Pt switches [30], [31] were fabricated on-chip (Fig. 3). Ag/SiO_2/Pt switches were chosen for their ease of fabrication and their compatibility with CMOS**.** Ag/SiO_2/Pt memory works by the creation and dissolution of a conductive Ag filament through the SiO_2, as shown in Fig. 4. When a positive voltage is applied to the Ag terminal, Ag is oxidized to form Ag cations that are dissolved into the SiO_2. The

electric field drives the Ag cations to the opposing Pt electrode, where they are reduced to form a Ag filament [32], [33].

First, Pt was patterned on top of the Al/Au/Pt pads to form the bottom electrode on the first terminals of the memristors. Active areas of the devices were defined by depositing a 200-nm conformal layer of SiO_2 via reactive sputtering and patterning 3-µm-diameter holes with a CHF_3 etch (windows on the second terminal were also etched in this step). A 16-nm-thick SiO_2 blanket layer was deposited via atomic layer deposition (ALD) at 300 °C. Ag was patterned as the top electrode and a blanket Ar mill was performed to remove the 16-nm-thick SiO_2 layer covering the second terminal of the memristors. To complete the switches, Au was patterned as a conductive bridge from the first to the second terminal. For comparison, Ag/SiO_2/Pt switches were also fabricated off-chip on a virgin Si wafer using the same processes and equipment as the on-chip switches. A diagram of the cross section of the devices is shown in Fig. 5 and a micrograph of the completed devices is shown in Fig. 6.

Chip packaging: After the Ag/SiO_2/Pt switches were fabricated, Au was patterned onto the bonding pads for easy wire bonding. The handle was diced down to 5 mm × 5 mm and the chip was mounted and wire bonded to a Kyocera LCC52 package (Fig. 7).

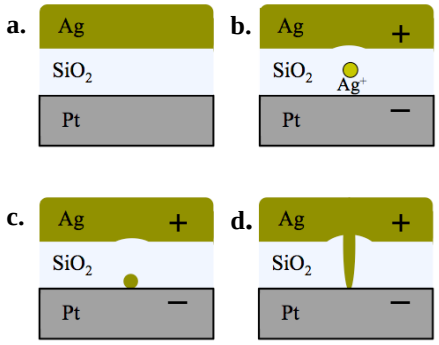

Figure 4. Schematic of Ag/SiO_2/Pt operating principle. The positive bias oxidizes Ag to yield Ag cations (b) that migrate to the Pt electrode where they are reduced (c) until a conductive Ag bridge is formed (d).

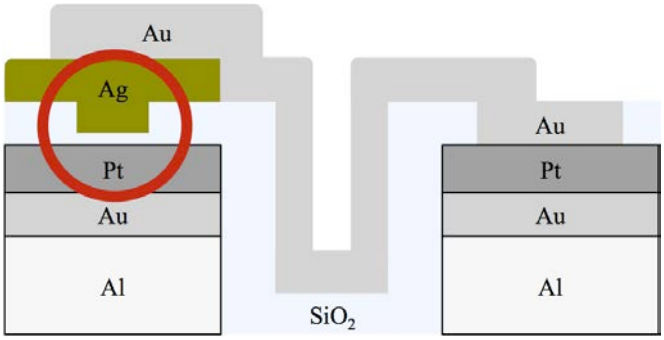

Figure 5. Cross-sectional diagram of fabricated structure with active Ag/SiO_2/Pt area circled. Optical micrograph of top view is in Fig. 6.

Results and Discussion

For characterization, voltages and currents were applied and measured using a Keithley 2401 voltage source and a LabVIEW interface was used to select memristors and save data. Testing of the switches on-chip showed that the Ag/SiO_2/Pt switches and the CMOS are functional (Fig. 8). 16 contiguous devices were selected at random to determine device yield. For all devices an initial read was performed at negative polarity (Fig. 8a), followed by a programming pulse at 5 V for 500 ms or a linear sweep to 5 V, followed by a second read applied after waiting 5 s. First, eight switches were programmed with a checkerboard pattern and read (Fig. 8b). Then the remaining eight switches were programmed and read (Fig. 8c) demonstrating a device yield of 81% (13 of 16). The 16 devices were also measured in parallel in sets of eight using 200 mV pulses using the internal read circuitry of the chip before and after being written to. These internal resistance measurements matched the measurements shown in Fig. 4.

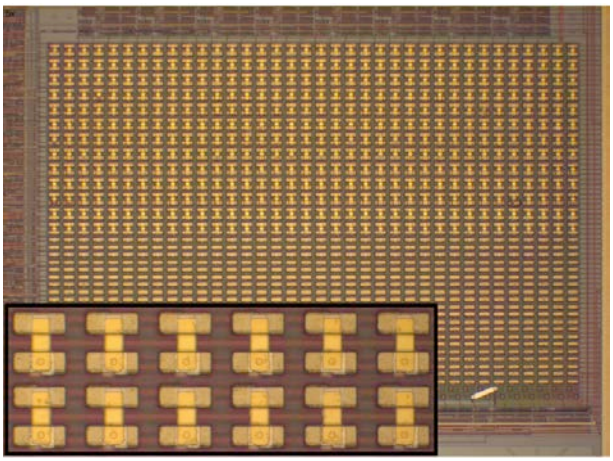

Figure 6. Device composition was varied row by row as the fabrication process was optimized. Inset shows devices on the two rows featured in this publication. Pad dimensions are 22 µm × 8 µm and 3-µm-diameter active device areas are visible on bottom rows.

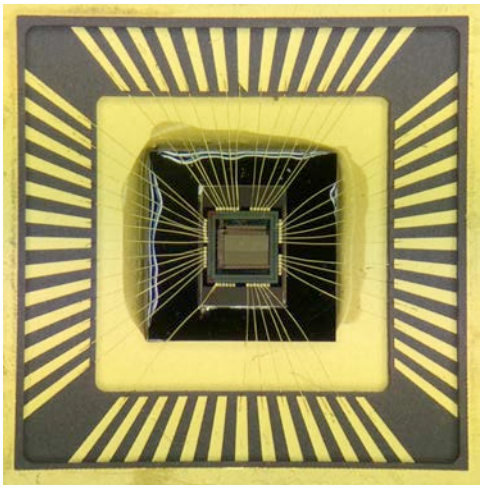

Figure 7. Fully packaged hybrid memristor/CMOS die in LCC52.

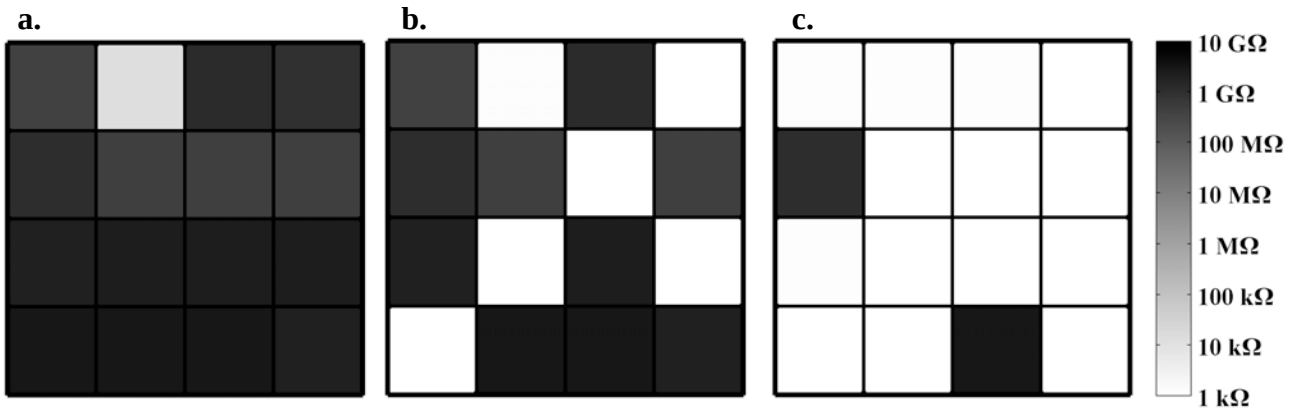

Figure 8. Device yield test. Measured resistance of 16 contiguous devices before (a) and after (b, c) 5 V was applied. A checkerboard pattern was programmed (b) followed by its complement (c). Notice one switch was initially shorted (a) and two switches did not change resistance (b and c), corresponding to a yield of 81% (13 of 16).

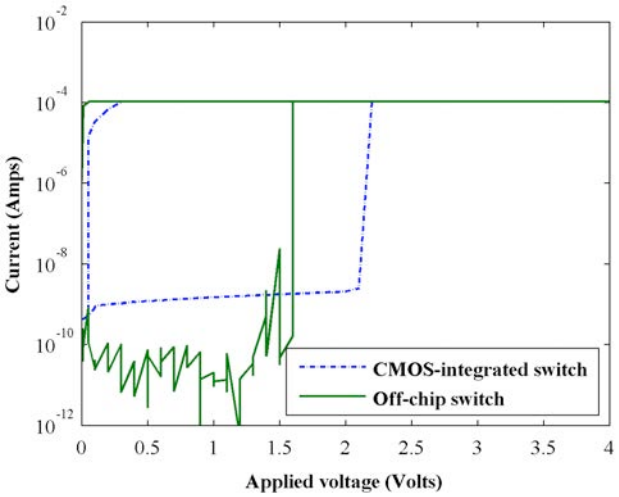

Figure 9. Typical positive voltage sweep for CMOS-integrated and off-chip memory. Devices integrated on CMOS have a minimum current level set by the CMOS circuitry.

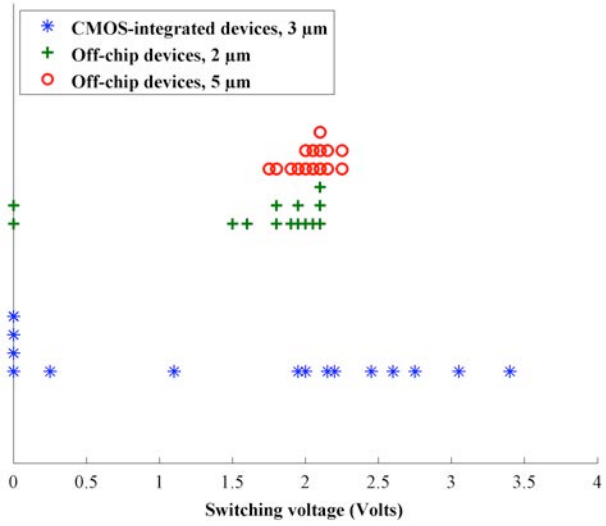

Figure 10. Scatterplot of switching voltages. Each dot represents one device. 3-µm off-chip devices were not available for comparison.

Another set of devices was chosen to determine the distribution of switching voltages by the application of a positive voltage sweep as in Fig. 9. The resulting scatterplot is shown in Fig. 10. The median switching voltages were similar, 2.0 V for off-chip devices and 2.1 V for vertically integrated devices. However, the spread in switching voltages was much larger for the set of vertically integrated switches. Presumably, this large spread was due to nonplanarity and nonuniformity of the 16-nm-thick active regions due to the large roughness of the Al pads relative to a virgin Si substrate. This issue would be resolved by fabricating the active regions of the devices on a BCB-planarized region in between the two Al pads.

Careful investigations revealed that for compliance currents between 1 nA and 1 mA, there was no negative polarity scheme that could reliably return the switches to a high resistance state. This stands in contrast to the reported literature [30], [31], [32]. It is hypothesized that the structure of the 16-nm ALD-SiO_2 contributed to Ag filament geometries that were too stable to be retracted in a reliable fashion at the compliance currents used. While there were differences in yield and switching voltage, there was no observed qualitative difference between vertically integrated memristors and devices fabricated off-chip.

Conclusions

We have presented and executed a hybrid integration scheme for post-CMOS vertical integration of memristors that is independent of CMOS die size. The process is versatile, allowing for different patterning techniques such as contact photolithography, electron beam lithography, and nanoimprint lithography with the use of a BCB planarization layer. As in this study, it is straightforward to make memristors with several different modifications on the same chip and later compare them in batch until the desired qualities are achieved. This can be of use to researchers looking to characterize one or several structures or looking to optimize a single device parameter using automated statistical measurements on large arrays of devices. Our approach is useful where small numbers of chips are desired, such as in niche applications or research.

Acknowledgments

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