Process Design Kit and Design Automation for Flexible Hybrid Electronics

Tsung-Ching Huang[1], Ting Lei[2,5], Leilai Shao[3], Sridhar Sivapurapu[4], Madhavan Swaminathan[4], Sicheng Li[1], Zhenan Bao[2], Kwang-Ting Cheng[3,6], Raymond Beausoleil[1]

[1]Hewlett Packard Labs, Palo Alto, USA
[2]Department of Chemical Engineering, Stanford University, USA
[3]Department of Electrical and Computer Engineering, University of California, Santa Barbara, USA
[4]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA
[5]Department of Materials Science and Engineering, Peking University, Beijing, China
[6]Department of Electric and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

Abstract

High-performance low-cost flexible hybrid electronics (FHE) are desirable for applications such as internet of things (IoT) and wearable electronics. Carbon-nanotube (CNT) thin-film transistor (TFT) is a promising candidate for high-performance FHE, because of its high carrier mobility, superior mechanical flexibility, and material compatibility with low-cost printing and solution-processes. Flexible sensors and peripheral CNT-TFT circuits, such as decoders, drivers and sense amplifiers, can be printed and hybrid-integrated with thinned (<50µm) silicon chips on soft, thin, and flexible substrates for a wide range of applications from flexible displays to wearable medical devices. Here we report: 1) process design kit (PDK) to enable FHE design automation for large-scale FHE circuits, and 2) solution-process proven intellectual property (IP) blocks for TFT circuits design, including *Pseudo-CMOS* [1] flexible digital logic and analog amplifiers shown in Figure 1. The FHE-PDK is fully compatible with silicon design tools for hybrid-integrated flexible circuits.

Author Keywords

Flexible hybrid electronics, thin-film transistors, thinned silicon

1. Introduction

Flexible and printable electronics have exponential growth in performance and cost reduction in recent years, which enables new applications such as disposable sensors, RFID tags, and low-cost internet of things (IoT) [2], [3]. To design a large-scale (>1,000 transistor count) digital and analog flexible TFT circuitry that is manufacturable with low-cost printing and solution-processes, however, is another story. Due to large printing process variations, as well as the lack of complementary and reliable TFTs, complex TFT circuits often suffer from high static power consumption and low circuit yields, particularly in low supply voltages, which make TFT circuits design a significant challenge.

On the other hand, the hybrid-integration of thinned silicon chips and printable TFTs on the same flexible substrate, emerges as a viable solution. The flexible sensors and TFT circuits that benefit from low manufacturing cost and conformal form factors can be an ideal complement to thinned silicon chips for designing a flexible IoT or wearable device. We have previously reported our progress of developing FHE-PDK [4][5] that include: 1) simulation models of printable passive and active devices, such as TFTs, resistors, inductors, and capacitors, 2) design rules of printable devices validated using specific printing or solution-process technologies, 3) multi-physics simulation models that can capture the interaction among electrical-thermal-mechanical performance, and 4) co-design capability for both printed electronics and thinned silicon chips, using the same design environment and EDA tool suites to ease the FHE design process.

Figure 1. Circuit design IP blocks, including *Pseudo-CMOS* [1] digital logic, analog amplifies, and passive elements (R/C). (Left) solution-processed CNT-TFT circuits on a 10µm flexible substrate for bending test, and (right) CNT-TFT circuits on the 1µm substrate.

In this paper, we report our latest progress regarding FHE-PDK to include: i) models of CNT, organic, and IGZO TFTs, CNT resistors, and parallel-plate capacitors, ii) experimentally-validated design rules and physical design verification capability, including design rule checking (DRC), layout-versus schematics (LVS) checking, and layout-parasitics extraction (LPE), and iii) low-voltage (3V) TFT digital and analog design IP. The technologies files, simulation models (SPICE and Verilog-A), and parameterized cells (p-cell) are fully compatible with mainstream EDA tools for silicon CMOS design, which makes FHE-PDK an ideal choice for co-design, co-simulate, and co-verify the FHE design containing both printed TFTs and silicon chips.

2. Device Modeling

Compact TFT Models: Several TFT compact models targeting specific technologies [6] have been developed in the past, which may not be generalized for other technologies. Some studies focus only on modeling the DC behavior [7], which doesn't support transient simulations. In this paper, we present a unified compact model of TFTs covering DC, AC and technology scaling factor for supporting FHE design, and also validate the proposed models against measurement results using three TFT technologies: carbon-nanotube (CNT) TFTs, indium-gallium-zinc-oxide (IGZO) TFTs and organic TFTs [4]. The model-measurement validation using current-voltage (I-V) curves is shown in Figure 2. Based on this model, we further perform circuit level validation based on fabricated *Pseudo-CMOS* [1] inverters, sequence generators and ring-oscillators. The proposed model is implemented using Verilog-A for SPICE co-simulations with silicon CMOS circuitry, thus enables FHE designers to explore TFT-CMOS flexible hybrid circuits and evaluate their performance for a wide range of commercial and military applications from sensing, display, IoT, healthcare, to wearable medical devices [4].

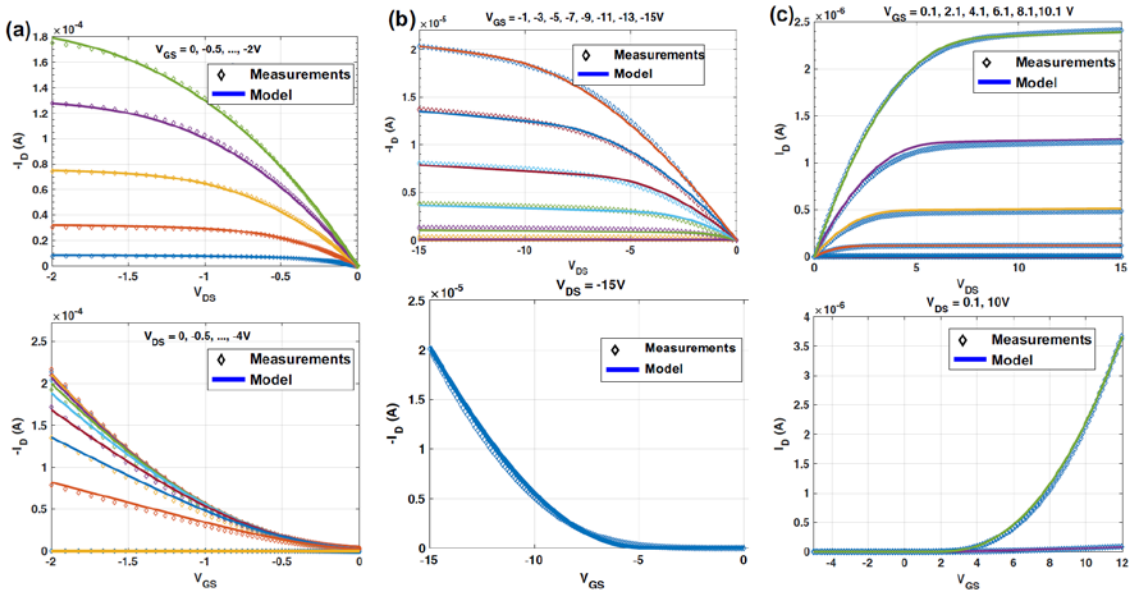

Figure 2. Measured (dotted) and fitted (solid) current-voltage (I-V) curves for (a) CNT-TFTs (W=125µm, L=25µm), (b) Organic TFT (W=5000µm, L=10µm), and (c) IGZO TFT (W=30µm, L=20µm) [4].

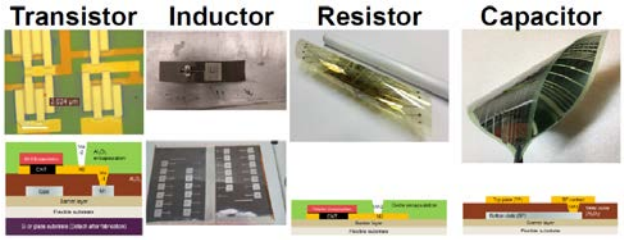

Figure 2. Flexible active and passive devices including CNT TFTs, spiral inductors, CNT resistors, and parallel-plate capacitors.

Resistor Models: In addition to TFTs, the CNT film can also be used to realize a linear resistor and the manufacturing process of a CNT resistor is fully compatible with CNT-TFTs. The CNT resistors have a wide range of applications such as linear and transimpedance amplifiers and low-pass filters etc. To further study the CNT resistor linearity and process variations, we fabricated and characterized 864 CNT resistors on a flexible substrate shown in Figure 2. With 40µm resistor width W, the length L is varied from 2µm to 100µm and the measured I-V curves are shown in Figure 3. CNT resistors show a good linearity when the length is greater than 10µm, when compared against a linear fitting curve. Figure 4 further reveals the process variations of the CNT resistors, where total 96 test samples are included for each test case of the resistor lengths L=10µm, 50µm, and 100µm, and total 384 test samples are included for the resistor length L=20µm. While the histograms follow Gaussian distributions, we can learn that the standard variations reduces when the resistor length L increases. The sheet resistance of the CNT film is around 137kΩ for L=10µm and decreases to 103kΩ for L=100µm. For the CNT resistors, the resistance values can be readily calculated using $R_{CNT} = R_{CH}*L/W_R+R_C/W_R$, where R_{CNT} is the total resistance in KΩ, R_{CH} is the channel resistance in KΩ, R_C in KΩ is the contact resistance attributed by metal-CNT interfaces, L is the resistor length in micrometers (µm) and W_R is the resistor width in micrometers (µm).

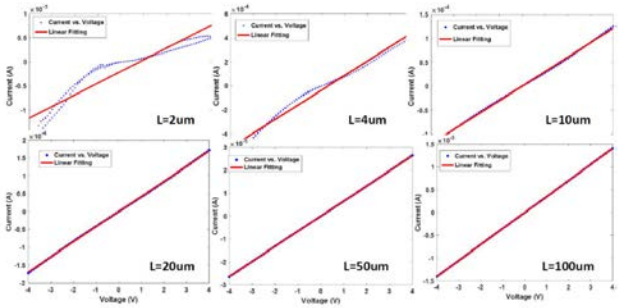

Figure 3. Measured current-voltage (I-V) curves (blue-dot) of CNT resistors against linear fitting model (red-line) for resistor length from 2µm to 100µm and the width is fixed to 40µm.

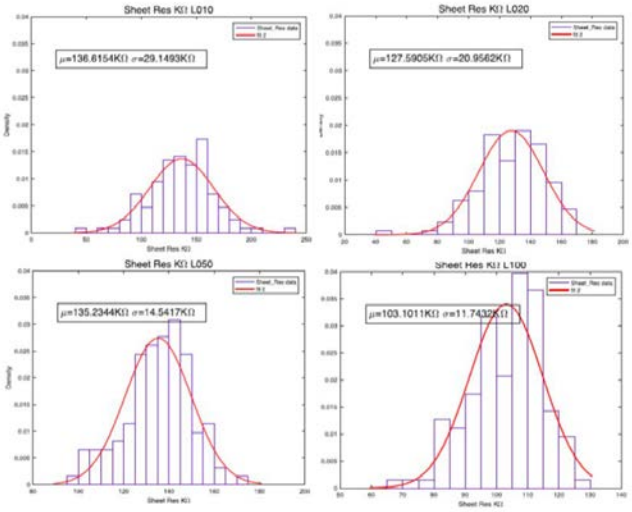

Figure 4. Measured statistical histograms of CNT resistors for resistor lengths from 10µm to 100µm and the width is fixed to 40µm.

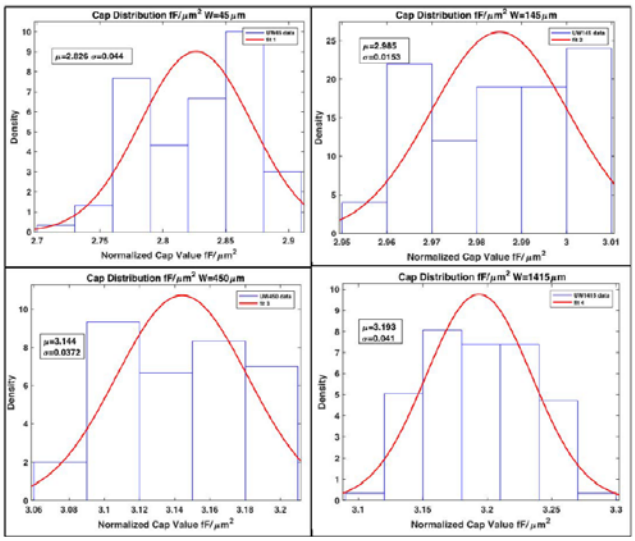

Figure 5. Measured statistical histograms of unit capacitance for the parallel-plate capacitors. The capacitor widths W_C are from 45μm to 445μm.

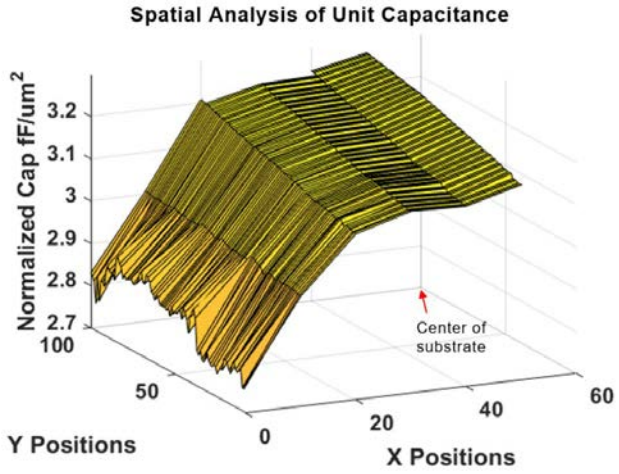

Figure 6. Measured 2D spatial analysis of the unit capacitance (fF/μm²) against the substrate dimensions in millimeters (mm).

Capacitor Models: In addition to CNT resistors, flexible capacitors can also be realized using TFT compatible solution-processes, for applications such as signal filters and equalizers. Here we use simple top-bottom parallel-plate structures to realize the flexile capacitors with 25nm thick Al_2O_3 dielectrics as shown in Figure 2. To further study the process variations of the capacitance, we designed and characterized 431 parallel-pate capacitors and the measurement results can be found in Figure 5 for the capacitor widths W_C from 45μm to 1415μm. We can learn that while the standard variations of the unit capacitance (~3fF/μm²) are similar among different capacitor widths W_C, the average unit capacitance increases with larger capacitor widths W_C. We attribute this phenomenon to thinner dielectrics for larger-sized capacitors. The 2D spatial analysis in Figure 6 shows the unit capacitance variations across the same flexible substrate, with which figure we can learn that the unit capacitance is higher at the center of the substrate. This could also be attributed to thinner dielectrics due to non-uniformity of the dielectrics thickness, which is often seen in solution-processes.

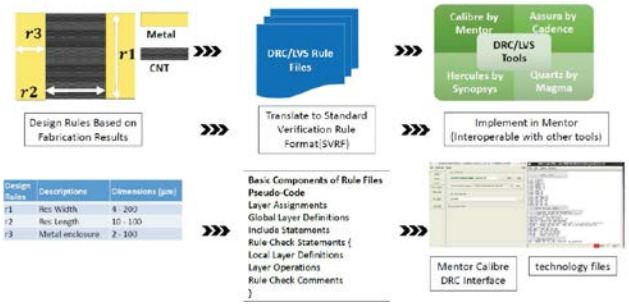

Figure 7. Physical verification flow (ex. DRC) for flexible devices such as a CNT resistor based on experimentally-validated design rules.

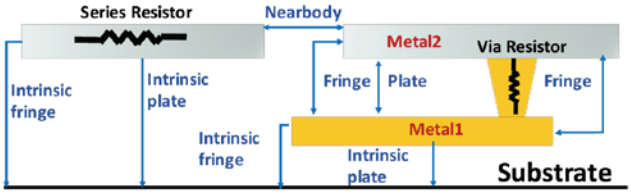

Figure 8. Parasitic resistance and capacitance that can be extracted using layout-parasitic-extraction (LPE) function with PDK.

3. Physical Design Verification

To enhance the productivity of FHE design, we incorporate mainstream silicon CMOS design tools for FHE-PDK design, simulation, and physical verification flow. We also create experimentally-proven design rules of CNT-TFTs, CNT resistors, parallel-plate capacitors using solution-processes, and design rules of spiral inductors using screen printing. Based on these design rules, we create technology files using Standard Verification Rule Format (SVRF), which is T-cl or Python based formats to perform physical verification using mainstream EDA tools such as Mentor Graphics *Calibre*. The physical design verification flow (ex. DRC) is illustrated in Figure 7. In addition to physical design verification, we also incorporate material properties to create technology files for layout parasitics extraction (LPE). Layout-related parasitics in flexible circuits can be significant compared with silicon chips, which is due to larger physical footprints. Thus, it is essential to include accurate estimates of layout-related parasitics such as resistance and capacitance for post-layout simulations, particularly for high-performance FHE circuits. As shown in Fig. 8, the parasitic capacitance including intrinsic and fringe capacitance can be derived using the mainstream LPE tools with the knowledge of material properties such as dielectric constants and dielectrics thickness etc, as well as the physical design dimensions. Parasitic resistors are mainly attributed to metal layers as well as the layer-to-layer VIAs. After the parasitics extraction and back-annotation to the circuit netlist, post-layout simulations can be performed to include the layout-dependent parasitics for simulating flexible circuits.

4. Foundational Design IP

Digital Logic: Complementary circuit with both p and n-types of transistors are essential in silicon CMOS design to reduce the static power consumption as well as to improve the noise margin. However, certain TFT technologies such as IGZO and amorphous silicon do not offer good complementary devices which makes low-power and robust TFT digital design difficult. To overcome

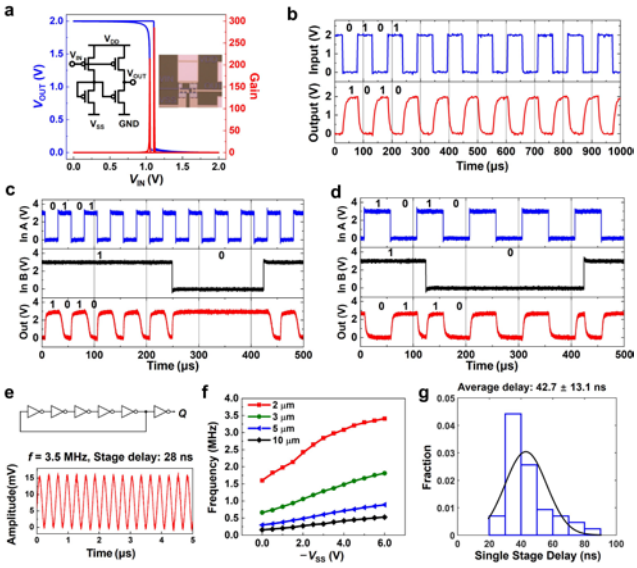

Figure 9. (a) Measured input-output transfer curve and schematics of a *Pseudo-CMOS* inverter. (b-d) measured waveforms of *Pseudo-CMOS* inverter, NAND, and XOR logic gates. (e) measured waveforms of a 5-stage ring oscillator with a large output load 125pF. (f) voltage dependency of the 5-stage ring-oscillator frequencies on the terminal VSS. (g) histogram of the stage-delay using forty-four 5-stage ring-oscillators. The average stage delay is 42.7ns.

the design challenges such as the lack of complementary reliable TFTs as well as large process variations for printed and solution-processed TFT circuits, we have previously reported a robust design style *Pseudo-CMOS* [1]. Based on *Pseudo-CMOS*, we have developed a variety of solution-process proven digital logic design IP blocks ranging from a simple inverter, simple logic gates to linear-feedback shifter registers (LFSR) using CNT-TFTs. With the aid of FHE-PDK, we can now design, simulate, and verify a complex TFT digital circuit block with thousands of CNT-TFTs within a short period of time. The simulated performance and power also provide a good correlation with the fabricated CNT-TFT circuits at low supply voltages (3V).

Signal Amplification: In addition to digital logic, we also develop analog design IP such as variable gain amplifier (VGA) that is commonly used in sensor interfaces to provide signal amplifications. The schematics and measured input-output waveforms of a 9T-1C VGA is shown in Figure 10. The voltage gain of the VGA can be tuned by varying the gate voltage VTUNE of the feedback TFT. The physical size of the 9T-1C amplifier is 350x350 μm^2 including a parallel-plate input capacitor to attenuate low-frequency input noises and block the dc current feedback to the input terminal. The gain-bandwidth of the VGA can be tuned from 32dB gain with 33 KHz bandwidth to 60dB with 15KHz bandwidth by varying VTUNE voltages, and the minimum input signal can be as small as 5mV.

5. Conclusion

In this paper, we report our latest development of FHE-PDK for FHE design, simulation, and physical design verification. While FHE is emerging as a viable solution for high-performance low-cost IoT and wearable applications, the device models, design rules, and technology files are still missing to enable the co-design

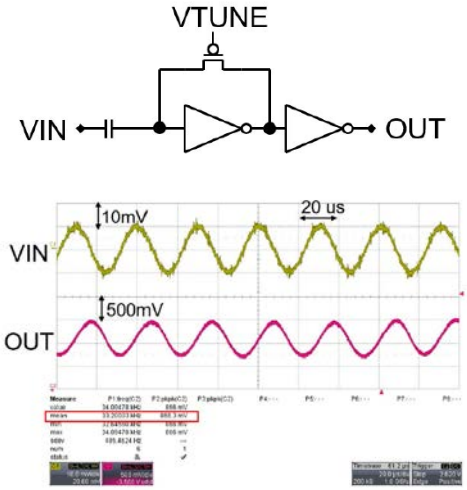

Figure 10. Measured input-output waveforms of a 9T-1C *Pseudo-CMOS* inverter-based VGA with CNT-TFTs.

and co-simulations of flexible TFT circuits and thinned silicon chips. FHE-PDK fills these gaps by experimentally-validated models, design rules, technology files, P-cells, and digital/analog design IP blocks. We believe that FHE-PDK will emerge as the must-have toolbox for FHE designers.

6. Acknowledgement

This material is based, in part, on research sponsored by Air Force Research Laboratory under agreement number FA8650-15-2-5401, as conducted through the flexible hybrid electronics manufacturing innovation institute, NextFlex. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of Air Force Research Laboratory or the U.S. Government. The authors would also like to thank Prof. Ta-ya Chu and Prof. Man Wong for their contributions.

7. References

[1] T. Huang et al, "Pseudo-CMOS: A design style for low-cost and robust flexible electronics," IEEE Transactions on Electron Devices, vol. 58, no. 1, pp. 141–150, January 2011.

[2] S. Wang et al, "Skin electronics from scalable fabrication of an intrinsically stretchable transistor array," Nature 2018.

[3] K. Myny et al, "A flexible iso14443-a compliant 7.5mw 128b metal-oxide nfc barcode tag with direct clock division circuit from 13.56mhz carrier," in 2017 IEEE ISSCC, pp. 258–259.

[4] L. Shao et al, "Compact modeling of thin film transistors for flexible hybrid IoT design," in IEEE Design and Test of Computers 2019.

[5] L. Shao et al, "Process design kit for flexible hybrid electronics," in 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), 2018, pp. 651–657.

[6] O. Marinov et al, "Organic thin-film transistors: Part i–compact dc modeling," IEEE Transactions on Electron Devices, vol. 56, no. 12, pp. 2952–2961, 2009.

[7] J. Zhao et al, "Universal compact model for thin-film transistors and circuit simulation for low-cost flexible large area electronics," IEEE Transactions on Electron Devices, vol. 64, no. 5, pp. 2030–2037, 2017.