Compact Modeling of Thin Film Transistors for Flexible Hybrid IoT Design

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Abstract—Flexible Electronics (FE) is emerging for low-cost, light-weight wearable electronics, artificial skins and IoT nodes, benefiting from its low-cost fabrication and mechanical flexibility. Combining FE with thinned silicon chips, known as flexible hybrid electronics (FHE), can take advantages of both low-cost printed electronics and high performance silicon chips, which brings together flexible form factors and IoT innovations. Thin film transistors (TFTs), as a critical component for FHE applications, have achieved tremendous improvements in charge carrier mobility, device stability and scalability; however, an accurate compact model for TFTs which can capture fundamental behaviors of TFTs and be broadly applicable to multiple flexible technologies is still missing for circuit and system design. Such a model is crucial for designing flexible hybrid IoT (Flex-IoT) in order to enable design explorations and technology evaluations. In this paper, we present a SPICE-compatible unified compact model covering DC, AC and technology scaling of TFTs for Flex-IoT designs. We validated the presented model for three different types of TFT technologies and performed circuits-level investigations based on fabricated Pseudo-CMOS circuits. We demonstrate that the presented TFT model can provide accurate and trustworthy predictions for circuit evaluation and Flex-IoT system design.

Index Terms—Flexible hybrid electronics, Flex-IoT, thin-film transistors, compact model, Pseudo-CMOS, design automation.

I. INTRODUCTION

Flexible electronics is emerging as an alternative to conventional silicon electronics for applications such as wearable sensors, artificial skin, medical patches, bendable displays, foldable solar cells and disposable RFID tags [1][2]. Unlike conventional silicon electronics that needs sophisticated billion-dollar foundry for manufacturing, flexible electronic circuits can be fabricated on thin and conformable substrates such as plastic films, with low-cost high-throughput manufacturing methods such as ink-jet printing and roll-to-roll imprinting. The time-to-market as well as manufacturing cost can therefore be significantly reduced. Its flexible form factor also enables innovative designs for consumer electronics and biomedical applications [3][4].

However, circuit using pure flexible electronics suffers from slower operating speed and less reliability comparing to complementary-metal-oxide-semiconductor (CMOS) technology. For sensing applications, such as touch, temperature, sweat and bio-medical sensors [2], speed requirement is not critical and TFT technologies can operate at ~MHz range to support such applications. Printing or solution compatible processes make the integration between TFTs and sensors much easier and TFT itself also can be used for sensing [5]. Through heterogeneous integration of flexible devices and thinned silicon chips, we can bring low-cost sensing and high performance computing to various connected “things” for wearables and Flex-IoT sensing nodes. A conceptual Flex-IoT sensing node is illustrated in Fig. 1 where TFTs, sensors and thinned silicon chips are integrated on the same flexible substrate.

There exist several challenges before Flex-IoT can be broadly employed for next-generation wearable and IoT products. Due to material properties, TFTs are usually mono-type, either only p- or only n-type, devices [6]. Making air-stable complementary TFT circuits is quite challenging or often requires heterogeneous process integration of two different TFT technologies. Existing CMOS design methodologies for silicon electronics, therefore, cannot be directly applied for designing flexible electronics. Other factors such as high supply voltages and large process variations also make designing large-scale TFT circuits a significant challenge. To ease design challenges and perform technology evaluations, a trustworthy TFT compact model is needed to facilitate simulations and design explorations.

Several TFT compact models targeting specific technologies [7] have been developed in the past, which may not be generalized for other technologies. Some studies focus only on modeling the DC behavior [8], which doesn’t support transient simulations. In this paper, we present a unified compact model of TFTs covering DC, AC and technology scaling factor for supporting Flex-IoT design, and validate the model for three TFT technologies: carbon nanotube (CNT) TFTs, indium gallium zinc oxide (IGZO) TFTs and organic TFTs. Based on this model, we further perform circuit level validation based on fabricated Pseudo-CMOS inverters, sequence generators and ring-oscillators. The proposed model is implemented in Verilog-A which is compatible with SPICE simulation of
CMOS circuitry, thus enables designers to explore TFT based flexible hybrid circuits and evaluate their potentials. The rest of this paper is organized as follows: Section II provides observations and model derivations for TFTs; Section III demonstrates model validations against transistors and circuit measurements; Section IV investigates the technology scaling effect; Section V draws the conclusion.

II. UNIFIED TFT MODEL

A. Observations and Motivations

To investigate the effective mobility of fabricated TFTs, low source drain voltages ($V_{DS} = -0.5V$ and $V_{DS} = 0.1V$) are chosen for CNT-TFT and IGZO-TFT accordingly. The measured I-V curves are shown in the top part of Fig. 2 and the bottom part shows the effective mobility $\mu_{eff}$. From Fig. 2, we observed that the effective mobility $\mu_{eff}$ is enhanced as the $|V_{GS}|$ increases for both CNT-TFT and IGZO-TFT, when $|V_{GS}|$ is relative small. Similar mobility dependency phenomenon has been observed in OTFT and a-Si TFT [7], and the commonly accepted theories are based on charge drift in the presence of tail-distributed traps (TDTs) and variable range hopping (VRH) [7]. This common phenomenon among different TFT technologies encourages us to build a unified model to capture fundamental behaviors of different TFTs based on TDTs and VRH assumptions.

B. Assumptions and Analysis

1) Mobility Enhancement: Both theories indicate the field enhancement of the mobility:

$$\mu = \begin{cases} \mu_0(V_{G} - V_{th})^\gamma, & \text{N-type TFT} \\ \mu_0(V_{th} - V_{G})^\gamma, & \text{P-type TFT} \end{cases}$$

(1)

where $V_{th}$ is the threshold voltage, $\gamma$ is the field enhancement factor for mobility and $\mu_0$ is defined as the effective mobility when $|V_{G} - V_{th}| = 1$, as illustrated in Fig. 2(a). This mobility enhancement assumption explains the increase of the effective mobility at a low $|V_{GS}|$.

2) Contact Effect: The degeneration of mobility at high $|V_{GS}|$ can be explained partially by the contact resistances $R_S$ and $R_D$ at source/drain terminals, as shown in Fig. 3. These resistances result in effective gate-source/drain-source voltage drops: $V_{GS} = V_{GS} - R_SI_{DS}$, $V_{DS} = V_{DS} - (R_S + R_D)I_{DS} = V_{DS} - R_CI_{DS}$, where $R_C = R_S + R_D$ and the current with contact effect is denoted as $I_{DS}$. The derivations are not presented here for simplicity and the contact effect can be illustrated as follows:

$$I_{DS} \approx \frac{W C_{ox} \mu}{L(1 + kR_C(V_{GS} - V_{th}))} \{V_{GS} - V_{th} - \frac{1}{2} V_{DS}\}$$

(2)

$$\frac{I_{DS}}{\mu} = \frac{1}{1 + kR_C(V_{GS} - V_{th})} \quad k = \frac{W}{L C_{ox} \mu}$$

(3)

From Eq. (3), we can conclude that contact resistances lead to mobility reduction with a factor of $1/(1 + kR_C(V_{GS} - V_{th}))$ and it becomes more significant as $|V_{GS}|$ increases, which explains the degeneration of the effective mobility with a high $|V_{GS}|$ as shown in Fig. 2(a). For devices shown in Fig. 3, CNT-TFT has relative larger $k$ comparing to IGZO-TFT $k_{CNT} \approx 25k_{IGZO}$, thus leading to more obvious mobility degeneration.

3) Surface Roughness Effect: As gate voltage increases, electrons tend to flow closer the channel surface. Due to the low-cost fabrication process of TFTs, interface traps and surface roughness exist commonly leading to degeneration of the effective mobility [9]:

$$\frac{1}{\mu} = \frac{1}{1 + \theta |V_{GS} - V_{th}|};$$

(4)

Here, $\theta \approx 1/t_{ox}$ is a parameter related to the thickness of the gate oxide layer. This phenomenon combining with contact effect will lead to an overall mobility drop with a factor of $\approx 1/(1 + (\theta + kR_C)(V_{GS} - V_{th}))$. Although, surface roughness and contact effect have identical formula with a term proposal to $V_{GS} - V_{th}$, their physical explanations are different.

C. Model Derivations

We first establish the intrinsic current model based on the mobility enhancement assumption, then extend the model to capture parasitics and second order effects.

1) Intrinsic Current Model: We integrate the mobility enhancement assumption Eq. (1) with the n type charge drift model of Eqs. (5) - (7) to derive the intrinsic current model [7]:

$$I_{DS(n)} = Q_C h(x)v; \quad v = u_{eff} \frac{\partial V(x)}{\partial x}$$

(5)

$$Q_C h(x) = W C_{ox}(V_{G} - V_{th} - V(x))$$

(6)

$$u_{eff} = \mu_0(V_{G} - V_{th} - V(x))$$

(7)
Since the current is constant in the channel [9], integrating along the channel \( \int_{x=0}^{L} I_D(x)dx \) yields:

\[
I_D = \frac{k}{(\gamma + 2)} ((V_{GS} - V_{th})^{\gamma + 2} - (V_{GD} - V_{th})^{\gamma + 2}) \tag{8}
\]

where \( k \) is defined as \( \frac{WC_{ox} \mu}{L} \). Similar to metal-oxide-field-effect-transistor (MOSFET), we divide Eq. (8) into two regions: 1) linear region, and 2) saturation region. Applying the Taylor expansion and keep the first and second order terms, we can then simplify the formula as:

\[
I_D \approx \begin{cases} 
\frac{k'}{\gamma + 2} (V_{GT} - \frac{1+2}{2} V_{DS}) V_{DS}, & V_{DS} \leq V_{GT} \\
 k' V_{GT}^2; & V_{DS} > V_{GT} 
\end{cases} \tag{9}
\]

\[
k' = k V_{GT}^2; V_{GT} = V_{GS} - V_{th} \tag{10}
\]

Notice that Eq. (9) becomes a conventional MOSFET model when \( \gamma = 0 \). This is because the main difference between the TFT intrinsic model, Eq. (8) and the MOSFET model is the mobility enhancement dependency on the gate voltage. This inherent connection between Eq. (9) and the MOSFET model leads to a major advantage: we can readily include second-order effects, such as channel length modulation, taking advantage of mature MOSFET theories.

2) Extending the Intrinsic Model: To further enrich the capability of the TFT intrinsic model, we incorporate the channel length modulation \( 1 + \lambda V_{SD} \) and surface roughness effect into Eq. (8) and the limiting function \( f_{lim}(V_G, V) \) is added to provide smooth transitions between the sub-threshold region and the above-threshold region [9]:

\[
I_D = \frac{k' \beta}{\gamma + 2} (f(V_G, V_3)^{\gamma + 2} - f(V_G, V_D)^{\gamma + 2})(1 + \lambda V_{DS}) \tag{11}
\]

\[
f_{lim}(V_G, V) = SS \ln[1 + \exp(\frac{V_G - V_{th} - V}{SS})]; \beta = \frac{1}{1 + \theta V_{GT}} \tag{12}
\]

where \( \lambda \) is the channel length modulation factor and \( SS \) is related to the sub-threshold slope.

3) Extrinsic Contact Resistance: Two series resistances \( R_s \) and \( R_D \) are added to account for the contact effect as shown in Fig. 3. To accurately extract the contact resistance, we apply transmission line method (TLM) to \( \sim 500 \) fabricated CNT based devices, as shown in Fig. 4. The total resistance \( R_{total} \) of the two terminal test structure is composed of contact resistance \( R_c = R_{res} + R_{cd} \) and channel resistance \( R_{ch} \). Here, \( R_{ch} \) is the sheet resistance of the channel and \( R_c = R_{cd} + R_{res} \) is the unit width contact resistance.

\[
R_{total} = \frac{R_c}{W} + \frac{R_{ch} L}{W} \tag{13}
\]

Eq. (13) indicates that the \( R_{total} \) is a linear function of \( L \) if \( W \) is kept as a constant. Fig. 4 contains two critical parameters: 1) unit width contact resistance \( (R_c/W = 4.78 K\Omega) \) can be extracted from the intersection when \( L = 0 \); 2) the minimum width \( W_{min} \approx 2 \mu m \) required for source/drain terminal can be extracted from the intersection when \( R_{total} = 0 \). The extracted contact resistance will be used in our model and \( W_{min} \) for source/drain terminal will guide the device fabrications.

4) Gate Capacitance: Two lumped capacitors \( C_{GS} \) and \( C_{GD} \) are added to characterize the transient behavior of the TFT circuits. Due to the large device sizes (hundreds of \( \mu m \) scale), two lumped capacitors are sufficient accurate to capture the transient responses of TFT circuits. Gate source/drain parasitic capacitors \( C_{GSO} \) and \( C_{GDO} \) are also included to improve the accuracy.

\[
C_{GS} = C_{GCS} + C_{GSO}; C_{GD} = C_{GCD} + C_{GDO}; \tag{14}
\]

\[
C_{GCS} = \frac{C_{ox} W L}{3} \left[ 1 - \frac{V_{GT} - V_{DS}}{2 V_{GT} - V_{DSe}} \right]^2 \tag{15}
\]

\[
C_{GCD} = \frac{C_{ox} W L}{3} \left[ 1 - \frac{V_{GT} - V_{DSe}}{2 V_{GT} - V_{DSe}} \right]^2 \tag{16}
\]

\[
V_{DSe} = \frac{1}{2} \left[ V_{DS} + V_{GT} - \sqrt{V_{DS}^2 + (V_{DS} - V_{GT})^2} \right] \tag{17}
\]

where \( L_{gs} \) is the gate source/drain overlap and \( V_0 \) is a small number (\( \sim 10 mV \)) to improve convergence. \( C_{GCS} \) and \( C_{GCD} \) are adapted from the Meyer capacitance model and typical gate voltage dependent behaviors are shown in Fig. 7(a). The final equivalent circuit model is shown in Fig. 5 and all equations can be implemented in Verilog-A for SPICE simulations.

III. MODEL VALIDATIONS

In this section, we compare the SPICE simulation results with measured drain-source current versus gate voltages (I-V) curves from CNT-TFT, IGZO-TFT and OTFT. And circuit level validations are performed with fabricated Pseudo-CMOS inverters and ring-oscillators [1].

A. Device Validation

We first examined the unified TFT compact model with three measured I-V curves from CNT, IGZO and Organic TFTs. It can be seen that the model is able to accurately predict the dc behaviors of different TFTs, which well demonstrate the broad applicability of the unified compact model. The excellent match between model predictions and measurement data further confirm the validity of the above-mentioned model derivations and assumptions. We extracted model parameters for three types of TFTs listed in Table 1. For CNT-TFTs, 52 devices’ statistical information are also included and a Gaussian distribution is assumed for process variations, where the mean value \( \mu \) and standard deviation \( \sigma \) are shown.

Field effect mobility extracted based on an idealized MOSFET current model has been widely used for TFT performance
benchmarking. With the field-dependent properties, the extracted mobility could vary significantly at different effective gate voltage bias. Therefore, to fairly evaluate the performance of a TFT, combination of the low field effect mobility ($\mu_0$) and field-dependent factor ($\gamma$) should be used to fairly evaluate the mobility performance. Thus, the unified compact model enables accurate simulation and also serves as a benchmark for technology evaluations.

**B. Circuits Validation**

Beside single devices, the model must be able to predict the circuit level behaviors with high accuracy. We therefore compare the SPICE simulation results with the measured voltage transfer curves (VTCs), rising/falling times and ring-oscillator’s waveform.

1) **Introduction to Pseudo-CMOS:** Pseudo-CMOS is a design style proposed to address challenges of TFT circuit design based on mono-type devices [1], which has been proven a robust design style for flexible digital, analog, and power circuits. Compared to conventional mono-type design styles, such as the diode-load or resistive-load designs, Pseudo-CMOS offers better noise margin and provides post-fabrication tunability at the cost of an additional power rail $V_{SS}$. There are two topologies of Pseudo-CMOS: depletion (Pseudo-D) and enhancement (Pseudo-E) type. Both Pseudo-D and Pseudo-E inverter’s schematics are shown in Fig. 6(a) and (b), which consists of three power rails, $V_{DD}$, $V_{SS}$ and GND, and four transistors $M_1$-$4$.

2) **VTC Validation:** In Fig. 6(c), we compare the SPICE-simulated voltage transfer curves (VTCs) with actual measurement data, where solid lines are SPICE simulations and dots are measurements. Simulated VTCs match closely with the circuit measurements over a wide range of supply voltages $V_{DD}$, from 0.8V to 1.6V. Despite minor discrepancies in low supply voltages, the proposed model accurately predicts the DC behaviors of a Pseudo-D inverter. In Fig. 6(d), 26 pseudo-D inverter’s VTCs are plotted together and the SPICE simulations (bold lines) can accurately predict the average behaviors of the VTCs using the mean values in Table I.

3) **Dynamic Validation:** We validated our AC model using the Pseudo-CMOS inverter’s rising/falling times, ring-oscillator’s measured waveforms and sequence generator’s dynamic behaviors. As shown in Fig. 7(b), with the developed DC model and capacitance model, the transient simulation result well captures the oscillation frequency and the amplitude compared with the measurement data. To analyze the wafer
level variations, we first conducted a case study on the Pseudo-E inverter’s dynamic behaviors after taking variations into considerations. Monte Carlo simulations were performed with standard variation summarized in Table I of CNT-TFTs. As shown in Fig. 6(e)-(h), our model can indeed capture the dynamic behaviors and variations of Pseudo-E inverters, as evident by good match to results of fabricated CNT-TFT based devices. Also, we designed and tested 34 five-stage ring oscillators in a 4-inch wafer with their statistics summarized in Fig. 7(c). 500 Monte Carlo simulations are performed with the developed model and statistical simulation results show less than 10% errors comparing to physical measurements as indicated in Fig. 7(c)-(d). These errors are mainly caused by device and interconnect parasitics, which will be discussed in the next section and could be a very important future work. Furthermore, we designed, fabricated and tested a linear feedback shift register (LFSR) based sequence generator, which can be applied in signature generation, cryptography and test-patter generation, as shown in Fig. 7(e)-(f). The sequence generator contains more than 100 CNT-TFTs and our model is able to accurately predict the outcome of such a medium scale circuit, as indicated in Fig. 7(g), which further demonstrates our model’s capability to predict relative complex circuitry’s behaviors.

At the device level, validations have been conducted for three different TFT technologies. At the circuit level, we compared the model predictions with fabricated Pseudo-CMOS circuits. In summary, the good match between model and measurements of both DC and transient simulations indicate that the developed unified TFT model can accurately predict both device and circuit level behaviors.

### IV. TECHNOLOGY SCALING

In this section, we further investigate the channel length scaling effect.

First, we compared the model predictions of a Pseudo-D inverter with measurements of 6 fabricated circuits with channel length of $3 \mu m$. As shown in Fig. 8(a), the comparison between the DC simulation and the circuit measurements for Pseudo-D inverters shows a good correlation for channel length down to $3 \mu m$. For AC behaviors, a 5-stage Pseudo-E based ring-oscillator is used as a vehicle for investigating the scaling effect. Both model predictions and measurements of ring-oscillator’s frequency are shown in Fig. 8(b). Both simulations and measurements show that frequency does not increase quadratically as channel length decreases. This is because the non-negligible device parasitics, such as contact resistance and parasitic gate capacitance. Another observation is that as channel length decreases, the deviation of model predictions from the measurements grows. This phenomenon is due to non-trivial interconnect parasitics. For instance, a printed wire’s sheet resistance could be as large as $\sim 1 \Omega/\square$. Also, typical TFT process only has 2-3 metal layers, which inevitably will increase the overlap between layers causing significant parasitic capacitance. Thus, for high performance TFT circuit design, accurate interconnect model and layout parasitic extraction are necessary to better capture the circuit behaviors. This would be an important subject of future study to further improve the accuracy of the simulation results.
Fig. 7: (a) Meyer capacitance model for p-type devices; (b) SPICE simulated five-stage ring-oscillator’s waveform vs. measured waveform; (c) 34 measured 5-stage Pseudo-D ring oscillators’ stage delay; (d) 50 Monte Carlo simulations of ring oscillators’ stage delay; (e)-(f) Schematic and die photo of a 3-bit maximum-length linear feedback shift register (LFSR) composed of three D-flip flops (DFFs) and one XOR gate; (g) Measurements and simulation results of a fabricated sequence generator (‘1110010’) with CLK=100 Hz, VDD=4 V and VSS=-4 V; (h) Waveforms of ring oscillators from 5 stages to 101 stages; (i) Simulated frequency and running time vs. ring oscillator’s stage with a total of 500 us simulation time and a 200 ns time step.

Fig. 8: (a) Dot lines: 6 CNT-TFT based Pseudo-D inverter’s VTCs with channel length \( L = 3\mu m \); solid line: model predictions for Pseudo-D inverter; (b) Model prediction of CNT-TFT based 5-stage ring-oscillator’s frequency vs. measured frequency.

V. CONCLUSION AND FUTURE WORK

In this paper, we present a unified TFT model for flexible hybrid IoT circuit and system design. The proposed model has been validated using three different TFT technologies and several Pseudo-CMOS circuits, covering both DC and AC behaviors. Also, we investigate technology scaling effect with channel scaled from 25\( \mu m \) to 3 \( \mu m \). The analysis and measurement indicate that device parasitics should be carefully optimized to approach the ideal quadratic improvement with channel length scaling. We further identify that interconnect parasitics should be included to further improve the simulation accuracy.

REFERENCES