Spatial Pattern Analysis of Process Variations in Silicon Microring Modulators

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***Abstract*—We identify significant spatial patterns in the wafer-scale process variation data of silicon microring modulators. These spatial patterns implicate some variation sources in certain fabrication process steps.**

Keywords— Process variation, silicon photonics, microring modulator

I. INTRODUCTION

Silicon photonics is highly attractive in short-reach optical interconnects because of its CMOS-compatibility, compact footprint, and energy efficiency [1]. However, as the device dimensions are in submicron era, the compact silicon photonic devices suffer from significant fabrication process variations, which would impair the optical interconnect system's performance without proper control methods being taken [6].

Process variations of silicon photonic devices have been studied in many previous work such as [2][3], which, however, did not systematically analyze the spatial patterns in the process variations. In this work, we quantitatively analyze the spatial patterns in the wafer-scale variations of microring modulators' performance and local heaters' resistance. The wafer-scale measured data is decomposed into two spatial pattern components, which are very valuable in analyzing the process variation sources and improving the fabrication steps.

II. DEVICE GEOMETRY AND MODEL

The microring modulators with 5 μm radius are fabricated on 8-inch silicon-on-insulator (SOI) wafers. There are 61 full dies (20 mm x 20 mm) on one wafer. The 250 nm silicon layer is dry etched to 50 nm, forming the rib waveguide. Then the inner and outer regions of the microring are doped at $3\times10^{19}\,\mathrm{cm}^{-3}$ with P and N implantation, respectively (Fig. 1 ab). A square region inside the microring is also P-doped at the same implantation step to construct a local heater in order to thermally tune the microring's resonance wavelength.

A small signal circuit model for this PIN junction microring modulator is shown in Fig. 1 (c), where the R_D and C_D represent the resistance and capacitance of the PIN diode [4]. This small signal model well captures the high-speed performance of the microring modulator [5]. The model parameters are extracted from the S11 test of the microring modulator, and could be used to calculate the RC-limited modulation bandwidth of the modualtor [4][5].

III. SPATIAL PATTERN DECOMPOSITION AND ANALYSIS

We first measure and then decompose the wafer-scale device characteristics. Though the resonance wavelength is a good fingerprint of the microring modulator, it requires additional efforts to track a specific resonance wavelength when the resonance wavelength drifts over one free spectral range (FSR) across the wafer. Therefore, as a proof of concept, we choose the electrical characteristics of the microring modulator that can be measured accurately and efficiently. We perform S11 test at 1 mA bias of the modulators. Then the S11 test data is fit into the small signal model with high accuracy [4] to extract the model parameters, among which the R_D is plotted in Fig. 2.

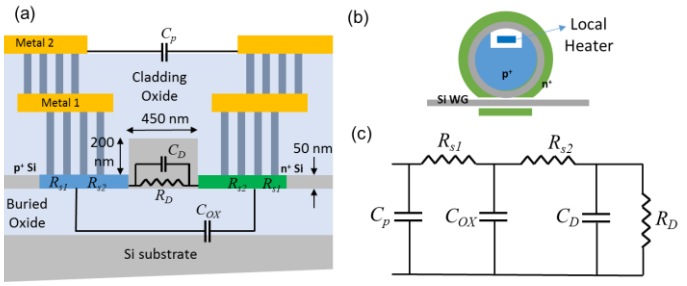

Fig. 1. (a) The cross section of the microring waveguide; (b) The planar view of the microring modulator and the local heater; (c) The small signal circuit model of the microring modulator.

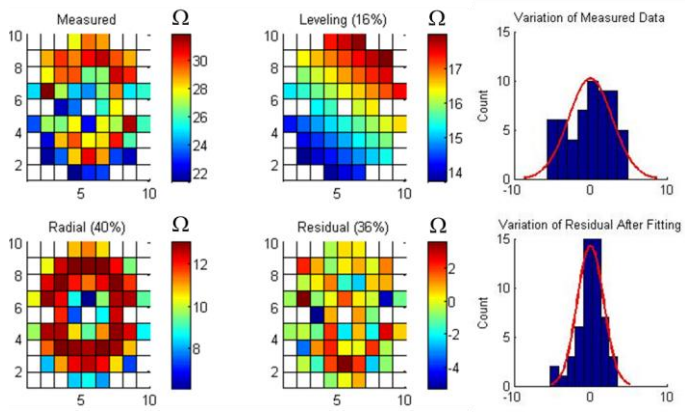

Fig. 2. Measured value and decomposition results of the diode resistance R_D. The center die is burnt. The radial component is not rotationally symmetric with respect to the wafer center since the DUT deviates from the die center.

The wafer-scale measured values are decomposed into the leveling component $ax+by$ and the radial component $c_1\sqrt{x^2+y^2}+c_2(x^2+y^2)$ as described by the following equation:

$$z_m(x,y)=ax+by+c_1\sqrt{x^2+y^2}+c_2(x^2+y^2)+d+\epsilon(x,y)$$

Where z_m is the measured value; x and y are the coordinates of the device-under-test (DUT) on the wafer with the wafer center as the origin; d is a constant representing the DC part in the measured value, which is included in the leveling component in the wafer-scale maps; ε is fitting error or the residual component. The weights of different components are evaluated by the variance of the component divided by the variance of the measured values. It should be noted that the sum of the weights of all the components is not necessarily one because the leveling and radial components are not orthogonal basis.

Using the decomposition approach above, all the extracted model parameters in Fig. 1 (c) are well explained by the two spatial components. Here we plot R_D in Fig. 2 as a representative due to space limitation, which shows significant leveling and radial components.

The RC-limited 3dB bandwidth of the microring modulator is calculated based on the small signal model parameters [4], as plotted in Fig. 3, which shows significant radial component and some leveling component.

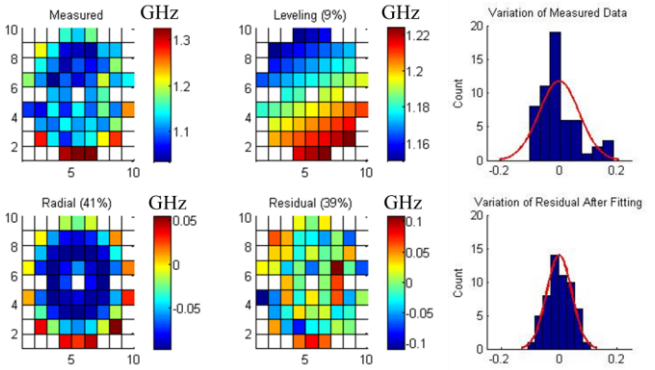

Fig. 3. Measured value and decomposition results of the wafer-scale RC-limited bandwidth.

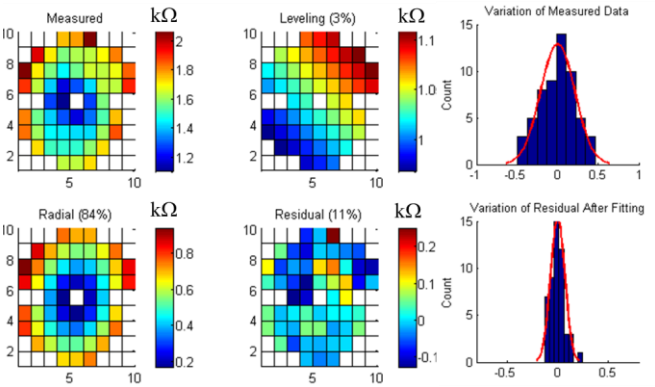

Fig. 4. Measured value and decomposition results of the wafer-scale heater resistance. (Three outlier dies are eliminated.)

We measure the local heater resistance by I-V test across the same wafer (Fig. 4). Good probe contact is confirmed by repeated measurements with repeating error less than 1 Ω. The decomposition of heater resistance data shows a significant radial component and a trivial leveling component.

IV. Implications on Fabrication Process Steps

The variation decomposition results show that the leveling component in C_D and R_D are respectively 15% and 16%, which are much larger than that in the local heater resistance (3%). Comparing to the local heater with simpler geometry, the modulator's PIN junction has additional dependencies such as the waveguide width (Fig. 1 ab). Therefore, the unique leveling component in the PIN junction's C_D and R_D is mainly introduced by the waveguide width variation, which is caused the imperfect leveling of silicon waveguide photomask during the lithography step.

Both the PIN junction's R_D and the heater resistance show significant radial patterns with higher resistance at the wafer edge. Additionally, the foundry measured SOI wafer thickness shows a radial pattern with 8 nm thicker at the wafer edge. Therefore, other contributors of the radial pattern, such as the silicon dry etch step and contact via etch step, also play important roles. Meanwhile, by noticing the weight percentages in Fig. 2, the contribution of the wafer thickness and the dry etch depth to the R_D's total variation effect is about 2.5 times (40% : 16%) as large as that of the leveling of the silicon waveguide photomask.

V. Conclusion

We have decomposed the wafer-scale process variation data of microring modulators and local heaters into two spatial pattern components (leveling and radial). The electrical characteristics of the modulator's PIN junction demonstrate both radial and leveling patterns, while the local heater resistances are dominated by the radial pattern. The spatial pattern analysis implicates variation sources of waveguide photomask leveling, SOI thickness, and the dry etch depth.

This work is limited to wafer-scale global variations due to the small number of DUTs on a wafer. With more dedicated test structures in future fabrication runs, and optical spectrum measurements, we can expect more accurate and informative analysis of both global and local variations using this approach.

Acknowledgment

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