ECE department, UCSB,
Santa Barbara, CA 93106
Cell: (805) 453-7678
ghofrani@ece.ucsb.edu

Amirali Ghofrani, Ph.D.

EDUCATION

- **Sep. 2010 – Mar. 2016**, **Ph.D. in Computer Engineering, University of California at Santa Barbara; GPA: 4.0**; Advisor: Prof. Kwang-Ting (Tim) Cheng.

  Ph.D. thesis: **"Towards Data Reliable, Low-Power, and Repairable Resistive Random Access Memories"**

  Memristor is an emerging resistive memory technology envisioned to replace flash memory as it offers non-volatile memory elements with fast access time, better-than-flash endurance, and ultra-high density.

  1) **Monitoring scheme to address write disturbance in access-transistor-free (ATF) memristive crossbars.**
     Proposed the use of two regular memristors to monitor the data degradation attributed to "write disturbance" in ATF memristive crossbars. The resistive crossbar was generated by a **skill** script. Monte Carlo simulation of disturbance accumulation was done in **C++**.
  2) **Write-time-variation-tolerant adaptive write scheme for ATF memristive crossbars.**
     The write circuitry and the memristive crossbar are implemented in **Cadence Virtuoso** and spice level simulation is performed to evaluate the feasibility and obtain energy saving merits of proposed method.
  3) **In-place repair for resistive memories utilizing Complementary Resistive Switches.**
     Low-cost dual-memristor-cells are proposed to repair stuck at ON defects in memristive memories, roughly doubling their lifetime. A statistical model was derived in **Mathematica** to evaluate the lifetime enhancement.
  4) **Associative memristive memory for approximate computing in GPUs.**
     Proposed the use of memristive memories along with GPUs to store and provide the results for frequent inputs at low energy costs. Further energy is realized by voltage overscaling, as the errors due to the *approximate* operation of the associative memristive memories in lower voltages are tolerated in multimedia applications, saving 2X on energy. The integration was modeled in **C++**.
  5) **A configurable CMOS memory platform for 3D integrated memristors.**
     Successful design and layout of a CMOS memory controller, taped out by MOSIS (collaborative effort).
  6) O**nline defect diagnosis of Network on Chip (NoC) interconnects**.
     End-to-end **ECC** is employed to detect and correct errors in a NoC distributed system. Error data is processed to derive a probabilistic model that locates the defective wires. Modeling and Simulations are done in **C++**.

- **M.Sc. in Computer Engineering, University of Santa Barbara, California, GPA 4.0.**
- M.Sc. in Computer Engineering, Computer Architecture, University of Tehran, Iran. GPA 3.91.

  Master thesis: **"Property Verification in TLM (SystemC) Designs"**
- B.Sc. in Computer Engineering, Hardware, University of Tehran, Iran. GPA 3.08.

COMPUTER SKILLS

- **Programming Languages**: C/C++, Java, CUDA, X86 and MIPS Assembly
- **Hardware Description Languages**: VHDL, Verilog, SystemC (TLM, RTL), SystemVerilog
- **Scripts**: TCL, Shell, Perl, Skill
- **EDA, IDE, and versioning Tools**: Microsoft Visual Studio, Eclipse, Intellij IDEA, Altera Quartus, Xilinx ISE, ModelSim, Cadence Virtuoso, Cadence Stratus, Synopsis Design Compiler, Cadence SoC Encounter, MATLAB, Mathematica, Mentor DFTAdvisor, Mentor FastScan, PODEM package, ZChaff SAT solver, Uppaal Timed Automata simulator, GIT, Perforce
- **Operating Systems**: Windows and Linux
- **Lab instruments**: Wide range of Oscilloscopes, Logic analyzers, and multi-meters

WORK & RESEARCH EXPERIENCES

- Sep. 10 – Now: Graduate Student Researcher, SOC Design and Test Lab, UCSB, Advisor: Prof. Tim Cheng
- Jun. 15 – Sep. 15: Interim Engr. Intern, **Qualcomm Atheros Inc.**, San Jose. Supervisor: Amitabh Menon
  - Implemented a data encryption module along with the interfacing logic inside the WiFi MAC (**SystemC)** and synthesized the module by Cadence Stratus **high-level synthesis** tool to get functional RTL. I also created comprehensive **test scenarios** for verification purposes.
- Jun. 12 – Sep. 12: **FPGA Intern**, Karl Storz Imaging Co., Goleta. Supervisor: David Demmin
  - Implemented a module to monitor, measure statistics, and manipulate video streams from an endoscope device in **Verilog**. The module was mapped on a Virtex-6 Xilinx FPGA.
- Sep. 07 – Sep. 10: Research Assistant, TLM lab, University of Tehran. Advisor: Prof. Z. Navabi
- Sep. 07 – Apr. 08: **FPGA Programmer**, Remote Systems Comm. Co., Tehran, Iran. Supervisor: M. R. Movahedi
  - Implemented the baseband parts of a spread spectrum radio frequency communication device in **VHDL**, including E1 channels multiplexer, framing, I-Q modulator and demodulator, ECC encoder and decoder (Reed-Solomon, Viterbi), and PLL adjustments on an Altera Cyclone-III FPGA device.
- Apr. 06 – May 07: **FPGA Programmer**, Rabi Kowsar Comm. Co., Tehran, Iran. Supervisor: Hossein Kalantari

SELECTED GRADUATE PROJECTS

- **Dual trail decomposition for VesFET realization of digital circuit using Genetic Algorithm (JAVA):** Given a net-list of transistors, genetic algorithm was employed to find the optimum-length dual trails to be placed on an array of VeSFET transistors to minimize the area. (UCSB, **Introduction to Design Automation**, fall 2011).
- **Observation Point Selection (JAVA, TCL):** Bio-inspired "Particle Swarm Optimization" algorithm was employed to select the best observation points in a digital design to give the highest test coverage. The process was automated using TCL programming to repeatedly call Modelsim simulation platform and open sockets to enable the communication between the JAVA programming platform and Modelsim (University of Tehran, fall2008 to spring 2009).
- **GPU-based parallelization of medical imaging pipeline (CUDA):** Implemented the denoising part of medical imaging pipeline to be executed on GPU (UCSB, **Applied Parallel Computing**, spring 2012).
- **ATPG (C):** Used a PODEM ATPG package in order to generate test inputs. The package was manipulated to use controllability and observability as a guide to choose the proper values for the nets (UCSB, **VLSI Testing Techniques**, fall 2010).
- **Superscalar processor with a hierarchical memory (Verilog):** Implemented a multi-issue (two instructions per clock cycle) MIPS processor, with two-phase clocking scheme. Tomasulo algorithm was employed to address data dependency hazards and a completion file is implemented to recover from exceptions. The memory hierarchy has two levels of 4-way set associative caches supporting MOESI coherency protocol, memory mapping unit, snooping, etc. (UCSB, **Advanced Computer Architecture**, winter 2011).
- **32Kb 250KHz subthreshold (350mV) SRAM (Cadence Virtuoso):** designed and implemented the subthreshold SRAM module with the required decoder, pre-charge and sense circuits, and 8T SRAM cells to work with 350mV supply voltage (UCSB, **High Performance Digital Circuit Design**, fall 2014).
- **Boundary Scan (VHDL):** Implemented full scan and boundary scan for an academic processor (UCSB, **VLSI Testing Techniques**, fall 2010).
- **NoC (VHDL):** Implemented a 3x3 NoC with an academic processor as the processing element (University of Tehran, **Digital design with VHDL**, spring 2009).

AREAS OF INTEREST

- **Resistive memories and data storage**
- **System modeling**
- **VLSI testing & verification**
- **FPGA and RTL implementation**
- **High level synthesis**

HONORS, AWARDS, AND RANKS

- 2011 **Best Student Paper Award**, International Test Conference (ITC)
- 2013 **Gerald W. Gordon Service Award**, IEEE Philadelphia Section & Test Technology Technical Council (TTTC) & International Test Conference (ITC)
- 2013 **GSA Dixon-Levy Service Award**, UCSB
- 2013 **Leslie Griffin Lawson Award for Outstanding Leadership**, UCSB
- 2015 **PhD Dissertation Fellowship Award**, Electrical & Computer Engineering Department, UCSB

SELECTED PUBLICATIONS

1. M. Lastras, **A. Ghofrani**, K.T. Cheng, "A Low-Power Hybrid Reconfigurable Architecture for Resistive Random-Access Memories", accepted in *IEEE Symposium on High Performance Computer Architecture (**HPCA**)*, Barcelona, March 2016.
2. **A. Ghofrani**, A. Rahimi, M. Lastras, L. Benini, R. Gupta, K.T. Cheng, "Associative Memristive Memory for Approximate Computing in GPUs", accepted in *IEEE Journal on Emerg. & Selected Topics in Circuits & Systems (JETCAS)*.
3. A. Rahimi, **A. Ghofrani**, K. T. Cheng, R. Gupta, "Approximate Associative Memristive Memory for Energy-Efficient GPUs", *Design, Automation, and Test in Europe **(DATE'15)***, Grenoble, France, March 2015.
4. **A. Ghofrani**, M. Lastras, S. Gaba, M. Payvand, W. Lu, L. Theogarajan, K. T. Cheng, "A Low-Power Variation-Aware Adaptive Write Scheme for Access-Transistor-Free Memristive Memory", *ACM Journal on Emerg. Tech. in Computing Systems (JETC)*, Vol. 12, Issue. 1, July 2015.
5. **A. Ghofrani**, M. Lastras, K-T. Cheng, "Toward Large-Scale Access-Transistor-Free Memristive Crossbars," *Asia South Pacific Design Automation Conference (ASPDAC'15)*, Tokyo, Japan, Jan 2015.
6. A. Rahimi, **A. Ghofrani**, M. Lastras, K.T. Cheng, L. Benini, R. Gupta , "Energy-Efficient GPGPU Architectures via Collaborative Compilation and Memristive Memory-Based Computing", *51st Design Automation Conference **(DAC'14)***, San Francisco, USA, Jun. 2014.
7. **A. Ghofrani**, M. Lastras, K-T. Cheng, "Towards Data Reliable Crossbar-Based Memristive Memories," *IEEE International Test Conference (ITC'13)*, USA, Sep. 2013.
8. **A. Ghofrani**, R. Parikh, S. Shamshiri, A. DeOrio, K-T. Cheng, V. Bertacco, "Comprehensive Online Defect Diagnosis in On-Chip Networks," 30th VLSI Test Symposium (VTS'12), USA, Apr. 2012.
9. S. Shamshiri, **A. Ghofrani**, K.T. Cheng, "End to End Error Correction and Online Diagnosis for On-Chip Networks", *IEEE International Test Conference (ITC'11)*, USA, Sep. 2011. **(Best Student Paper Award)**

ACTIVITIES

- **Journal and Conference Reviews:** IEEE Transactions on Nanotechnology (TNANO), IEEE Transactions on Computer (TC), Great Lakes Symposium on VLSI Systems (GLS-VLSI), Electronics & Telecommunications Research Institute Journal (ETRIJ), IEEE Journal On Emerging and Selected Topics in Circuits and Systems (JETCAS).
- **President of Iranian Graduate Student Association**, UCSB, June 2011-June 2013.
- Indoor soccer team captain: 3 Championships and 2 second places in UCSB intramural leagues.