Nicole Fern

nicole@ece.ucsb.edu

http://www.nicolefern.com

Current Employment

Appointed as a post-doc at UC Santa Barbara working with Prof. Tim Cheng until July 2018.

- **Citizenship:** United States

Research Interests

Hardware Security, Hardware Trojan Detection, Verification and Testing, Security at the Hardware/ Software Interface (device drivers, instruction set architectures, etc.)

Education

- **University of California - Santa Barbara** — Santa Barbara, California
  Postdoc Scholar: Electrical and Computer Engineering — *June 2016 – Present*
- **Hong Kong University of Science and Technology** — Hong Kong
  Visiting Scholar: Electrical and Computer Engineering — *August 2016 – November 2017*
- **University of California - Santa Barbara** — Santa Barbara, California
  MS/PhD Degree, Electrical and Computer Engineering — *September 2011 – June 2016*
  - Advisor: Professor Kwang-Ting (Tim) Cheng
  - SoC Design and Test Lab (http://cadlab.ece.ucsb.edu)
  - GPA: 4.0
- **The Cooper Union for the Advancement of Science and Art** — New York, New York
  Bachelor of Engineering, Electrical Engineering — *September 2007 – June 2011*
  - GPA: 3.9
  - Full-tuition merit scholarship

Recent Publications

- N. Fern and K-T. Cheng. "Mining Mutation Testing Simulation Traces for Security and Testbench Debugging", International Conference on Computer Aided Design (ICCAD), 2017.
- N. Fern, I. San, and K-T. Cheng. "Detecting Hardware Trojans in Unspecified Functionality Through Solving Satisfiability Problems", Asia South-Pacific Design Automation Conference (ASP-DAC), 2017.
- N. Fern and K-T. Cheng. "Verification and Trust for Unspecified IP Functionality" in *Hardware IP Security and Trust*, Prabhat Mishra, Swarup Bhunia, and Mark Tehranipoor, Eds. Springer, 2017.
- N. Fern, I. San, Ç. Koç, and K-T. Cheng. "Hiding Hardware Trojan Communication Channels in Partially Specified SoC Bus Functionality", IEEE Transactions on Computer-Aided Design of Integrated Circuits and System (TCAD), 2016.

- I. San, N. Fern, Ç. Koç, and K-T. Cheng. "Trojans Modifying Soft-Processor Instruction Sequences Embedded in FPGA Bitstreams", International Conference on Field-Programmable Logic and Applications (FPL), 2016.
- N. Fern, *Verification Techniques for Hardware Security*, PhD thesis, University of California, Santa Barbara, June 2016.
- N. Fern, I. San, Ç. Koç, and K-T. Cheng. "Hardware Trojans in Incompletely Specified On-chip Bus Systems", Design, Automation, Test in Europe (DATE) Conference, 2016.
- N. Fern and K-T. Cheng. "Detecting Hardware Trojans in Unspecified Functionality Using Mutation Testing", International Conference on Computer Aided Design (ICCAD), 2015.
- N. Fern, S. Kulkarni, and K-T. Cheng. "Hardware Trojans Hidden in RTL Don't Cares - Automated Insertion and Prevention Methodologies", International Test Conference (ITC), 2015.
- N. Lesperance*, S. Kulkarni, and K-T. Cheng, "Hardware Trojan Detection Using Exhaustive Testing of k-bit Subspaces", Asia South-Pacific Design Automation Conference (ASP-DAC), 2015.
- P. Lisherness, N. Lesperance*, and K-T. Cheng, "Mutation Analysis with Coverage Discounting", Design, Automation Test in Europe (DATE), 2013.

*Published under maiden name

Academic Research

- **Hardware Trojans in Unspecified Design Functionality** UC Santa Barbara
  Published in ITC, ICCAD, DATE, FPL, and ASP-DAC *PhD Student 2011 – 2016*
  - Unspecified functionality is a by-product of hardware implementation which an attacker can modify to leak information without detection by existing verification techniques
  - Developed attack scenarios for RTL Don't Cares (*ITC 2015*) and vulnerable unspecified functionality in on-chip bus systems (*DATE 2016*) and FPGA bitstreams (*FPL 2016*)
  - Provided methodologies to 1) **identify** unspecified and untested functionality vulnerable to Trojan insertion (*ICCAD 2015 & 2017*) and 2) **detect** Trojans in this highlighted functionality *without* requiring specification refinement (*ASP-DAC & ICCAD 2017*)
- **Hardware Trojan Detection Using Exhaustive Subspace Testing** UC Santa Barbara
  Published in ASP-DAC in 2015 *PhD Student 2011 – 2016*
  - Developed a post-silicon Hardware Trojan detection strategy based on the observation that an attacker is only able to use a small subset of design signals for Trojan triggering
  - Method targets exhaustive coverage of all possible subsets of signals the attacker could select instead of using controllability and observability metrics to bias testing
- **Coverage Discounting** UC Santa Barbara
  Published in DATE in 2013 *PhD Student 2011 – 2016*
  - Coverage Discounting uses mutation analysis to improve existing coverage metrics by accounting for the effectiveness of error propagation in the test bench
  - Evaluated Discounting technique on the OpenRISC and UART designs from OpenCores

Work Experience

- **Hardware Verification Engineer – Apple Inc.** Cupertino, California
  Silicon Engineering Group *Summer and Fall 2013*
  - Created a SystemVerilog testbench for a large design
  - Responsible for writing random and directed tests

- **Software Security Intern – Cisco Systems** Knoxville, Tennessee
  Cisco Security and Government Group *Summer 2012*
  - Created a code fuzzer for Multicast Source Discovery Protocol using the Peach fuzzing framework
  - Completed a series of practical applied security exercises
  - Learned to recognize and remedy common vulnerabilities in C programs

Skills

Programming Languages: C, SystemVerilog, Verilog, C++, Python, Perl, Matlab, x86, VHDL, MIPS

Computer Utilities: Unix Command Line, Git, Synopsys VCS, ModelSim, Yosys, Synopsys Design Compiler, ABC Logic Synthesis Tool, Certitude, GDB, Xilinx ISE Design Suite, Vivado, Flex, Bison, LaTeX, Octave

Activities and Academic Honors

- Selected to participate in the 2016 Rising Stars in EECS Workshop
- Received 3rd place in the E.J. McCluskey Doctoral Thesis Competition Semi-Finals
- Awarded the ECE Department Dissertation Fellowship for Spring 2016
- Teaching Assistant at UCSB for 6 academic quarters for courses requiring a weekly lecture (ECE154, Computer Architecture) and lab-based courses (ECE152A/B, students created hardware designs using a combination of FPGA boards and discrete circuit components) (2012 – 2015)
- Selected to teach a seminar on Matlab and also provide supplementary presentation of topics in signal processing and control systems (2010 – 2011)
- Winner of the Leon Machiz Prize for excellence in electrical engineering (2011)
- Winner of the Class of 1907 Award for the best enrolled or graduating student in calculus (2011)
- Winner of the Jesse Sherman Book Award for Outstanding Average in Electrical Engineering (2010, 2011)
- Dean's List at Cooper Union (8 consecutive semesters)