Fan (Fred) Lin

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Summary

PhD in developing state-of-the-art machine learning solutions for semiconductor manufacturing. Familiar with semiconductor production test flow and design for test (DFT), with a solid background in software programming.

Experience

Aug 2016 - Present	**Senior Hardware Engineer** Oracle, Santa Clara CA, USA Own a system that processes and analyzes semiconductor production test data for silicon debugging, process monitoring, and outlier detection. Develop a UI in JSP for data query and visualization.
Jun 2015 - Sep 2015	**Test Engineer Intern** Oracle, Santa Clara CA, USA Develop Perl scripts to enhance the system for handling test data. Implement a MATLAB GUI for visualizing and analyzing test data.
Jun 2013 - Sep 2013	**Research Intern** Broadcom, Irvine CA, USA Apply test data analytics for test cost reduction and test quality improvement.
Jul 2012 - Aug 2012	**Test Engineer Intern** Taiwan Semiconductor Manufacturing Company (TSMC), TAIWAN Maintain ATE control language (MTL) interface in Perl and develop test cost reduction methods.
	Teaching Assistant
Fall 2013	ECE 154A Introduction to Computer Architecture
Spring 2012, 13, 14	ECE 152A Digital Design Principles
Winter 2013, 14	ECE 15A Fundamentals of Logic Design

Education

Sep 2011 - Jun 2016	**MS/PhD in Computer Engineering** University of California, Santa Barbara	GPA 3.97/4
Sep 2006 - Jun 2010	**BS in Electrical Engineering** National Taiwan University, TAIWAN	GPA 3.84/4

Technical Skills

Skills	Data Analytics for Semiconductor Test and Validation Machine Learning and Artificial Neural Network DFT, VLSI Testing Tools and Techniques Digital VLSI Design and Embedded Systems Data Structure and Algorithms Software System (Data Pipeline) Development Excellent Problem Solving and Communication Skills
Programming	MATLAB, Verilog, C/C++/C#, Perl, Python, SQL, JSP, JavaScript
Software	Caffe, LIBSVM, Git, OpenCV, Quartus II, Virtuoso, ISE, ModelSim, Design Compiler, zChaff SAT solver, CUDD BDD solver, PODEM test generator, Linux

Publications

Jan 2017 **F. Lin**, K-T. Cheng, "An Artificial Neural Network Approach for Screening Test Escapes", *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan 2017.

Nov 2015 **F. Lin**, C-K. Hsu, A. G. Busetto, K-T. Cheng, "Pairwise Proximity-Based Features for Test Escape Screening", *International Conference on Computer-Aided Design (ICCAD)*, Nov 2015.

Oct 2015 **F. Lin**, C-K. Hsu, K-T. Cheng, "AdaTest: An Efficient Statistical Test Framework for Test Escape Screening", *International Test Conference (ITC)*, Oct 2015.

Nov 2014 **F. Lin**, C-K. Hsu, K-T. Cheng, "Learning from Production Test Data: Correlation Exploration and Feature Engineering", *Asian Test Symposium (ATS)*, Nov 2014.

Oct 2014 **F. Lin**, C-K. Hsu, K-T. Cheng, "Feature Engineering with Canonical Analysis for Effective Statistical Tests Screening Test Escapes", *International Test Conference (ITC)*, Oct 2014.

Mar 2014 S. Zhang, **F. Lin**, C-K. Hsu, K-T. Cheng, H. Wang "Joint Virtual Probe: Joint Exploration of Multiple Test Items' Spatial Patterns for Efficient Silicon Characterization and Test Prediction", *Design, Automation and Test in Europe (DATE)*, Mar 2014.

Sep 2013 C-K. Hsu, **F. Lin**, K-T. Cheng, W Zhang, X Li, J. M. Carulli, K. M. Butler, "Test Data Analytics - Exploring Spatial and Test-Item Correlations in Production Test Data", *International Test Conference (ITC)*, Sep 2013.

Honors

Mar 2016 **Dissertation Fellowship**
Awarded by the ECE Department of UC Santa Barbara based on thesis proposal.

Sep 2015 **Taiwan MoE Studying Abroad Scholarship**
Awarded by the Ministry of Education, Taiwan based on research performance.

Sep 2010 **Research Award**
Awarded by Lam Research Corp. for the implementation of a wide-range fast locking PLL.

Jun 2010 **Valedictorian Speech**
Invited for a speech on the 2010 commencement of the EE Department, National Taiwan University.

Jun 2010 **Presidential Award**
Awarded by the EE Department, National Taiwan University for top 10% GPA.

May 2010 **Innovation Award**
Awarded by National Taiwan University for the proposal of a hearing assisting system that employs voice recognition and a portable projector for output.

May 2010 **Special Project Award**
Awarded by National Taiwan University for the implementation of a wide-range fast locking PLL.

Selected Projects

2014 **Real-Time Pitch Shifter in Embedded System**
Developed a real-time pitch shifter on a Nexys 4 FPGA board.

2014 **Distributed ATM Simulators**
Implemented a 5-site ATM network using PAXOS for synchronizing the logs in Python.

2012 **Hardware Verification on OpenRISC1200**
Synthesized parts of OpenRISC1200, developed an RTPG, and simulated a miter circuit for functional verification.

2011 **PODEM Test Generator**
Modified PODEM in C based on various heuristics to improve fault coverage.

2009 **Microprocessor without Interlocked Pipeline Stages (MIPS)**
Implemented and simulated a pipelined MIPS in Verilog.

2008 **BDD Data Structure**
Implemented a BDD data structure with hash and cache in C++.