Yuyang Wang

Curriculum Vitae

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Educational Background

09.2015–Present **Ph.D. Student in Computer Engineering**, *University of California*, Santa Barbara, *GPA: 4.0/4.0*.
- Supervisor: Prof. Kwang-Ting (Tim) Cheng.
- Selected courses: Advanced VLSI Design, VLSI Project Design, Electronic and Photonic Integration and Packaging, Semiconductor Laser I, Introduction to Design Automation, VLSI Design Validaton.

09.2011–07.2015 **B.Eng. in Electronic Engineering**, *Tsinghua University*, Beijing, China, *GPA: 88/100*.
- Thesis: *The Separation Scheme of Control and Traffic Coverage in Hyper-Cellular Network for LTE: Design and Implementation,* Outstanding Thesis Award of the Department.

09.2013–12.2013 **Non-Degree Exchange Program**, *Korea Advanced Institute of Science and Technology (KAIST)*, Daejeon, Korea, *GPA: 4.12/4.3*.
- Exchange program among Tsinghua University, KAIST and Tokyo Institute of Technology under the CAMPUS ASIA Consortium.

Research Projects

09.2015–Present **Electronic and Photonic Design Automation (EPDA)**, *University of California*, Santa Barbara.
- Advisors: Prof. Kwang-Ting (Tim) Cheng, Prof. John Bowers, Prof. Nadir Dagli, & Prof. Clint Schow.
- Compact modeling and simulations of photonic devices and links with electronic driver circuits on multiple design automation platforms (Cadence Virtuoso, Synopsys Optsim, Lumerical Interconnect, & PhoeniX OptoDesigner).

09.2016–Present **System-level Simulation and Optimization of Optical Network-on-Chip (ONoC)**, *University of California*, Santa Barbara.
- Advisor: Prof. Kwang-Ting (Tim) Cheng.
- System-level simulations, design space explorations and design optimizations of on-chip optical links and networks based on models of real fabricated optical network-on-chips and realistic traffic patterns.

01.2017–Present **CMOS Driver Circuits Design for Lasers, Modulators and Optical Switches**, *University of California*, Santa Barbara.
- Advisor: Prof. Clint Schow.
- CMOS driver circuits design for directed-modulated lasers, high speed traveling wave Mach-Zehnder modulators and thermally tuned micro-ring based optical switches using 130 nm CMOS.

03.2016–06.2016 **Design of a Wireless Power Tranceiver in 0.5μm CMOS (Course Project)**, *University of California*, Santa Barbara.
- Advisor: Prof. Forrest Brewer.
- A DRC and LVS clean design of a wireless power tranceiver chip using 0.5 μm CMOS with a targeting frequency of 13.56 MHz, and the supplementary PCB board.

01.2016–03.2016 **Verilog Design Verification Using UVM (Course Project)**, *University of California*, Santa Barbara.
- Advisor: Prof. Li-C. Wang.
- Verification of typical APB2 and APB3 bus designs using Universal Verification Method (UVM).

01.2016–03.2016 **Area Minimized and Immortalized Wiring Topology for Electromigration Avoidance (Course Project)**, *University of California*, Santa Barbara.

- Advisor: Prof. Malgorzata Marek-Sadowska.
- Develop topology generation algorithms for area minimized and immortalized wiring topology for electromigration avoidance. Algorithms based on convex optimization and simulated annealing are investigated.

10.2014–06.2015 **Hyper-Cellular Mobile Communication System**, *Tsinghua University*, Beijing.

- Advisor: Prof. Zhisheng Niu.
- Design and implement the separation scheme of control and traffic coverage of the hyper-cellular network based on LTE protocols, where base stations (BS) are categorized into the signal BS which is always ON, and the data BS which can be switched to sleep mode for energy efficiency.

07.2014–09.2014 **Automated OS Level Device Runtime Power Management**, *Rice University*, Houston.

- Advisor: Prof. Lin Zhong.
- Modify HDL codes of three typical devices in SoC, prototype and verify one of the three methods proposed to substitute the current complicated Linux runtime power management framework, making power management of SoC devices much easier and independent of the drivers.

Professional Activities

07.2014–09.2014 **Student Intern**, *Rice Efficient Computing Group (RECG), Rice University*, Houston, Texas.

- Supervisor: Prof. Lin Zhong.
- Project: Automated OS Level Device Runtime Power Management.

04.2014–10.2014 **Translation of C. Hawkins, et.al., "CMOS Digital Integrated Circuits: A First Course" from English into Chinese**.

- Published by China Machine Press, Beijing, China in 2016.
- Proofread by Prof. Hong Chen.
- Translated the Preface and Chapter 1 through Chapter 9. Revised the translation of Chapter 10 through Chapter 12 translated by a collaborator.

05.2013–09.2013 **Translation of S. Kundu, et.al., "Nanoscale CMOS VLSI Circuits: Design for Manufacturability" from English into Chinese**.

- Published by Science Press, Beijing, China in 2014.
- Proofread by Prof. Xiaohong Wang.
- Translated the Preface and Chapter 1 through Chapter 4. Revised the translation of Chapter 5 through Chapter 8 translated by a collaborator.

Publications

Mar 2017 Rui Wu, **Yuyang Wang**, Zeyu Zhang, Chong Zhang, Clint L. Schow, John E. Bowers, and Kwang-Ting Cheng. "Compact Modeling and Circuit-Level Simulation of Silicon Nanophotonic Interconnects". *Design, Automation and Test in Europe (DATE)*, Lausanne, March 2017.

Jan 2017 Zeyu Zhang, Rui Wu, **Yuyang Wang**, Chong Zhang, Eric Stanton, Kwang-Ting Cheng, Clint L. Schow, and John E. Bowers. "Compact Modeling for Silicon Photonic Heterogeneously Integrated Circuits". Submitted to *Journal of Lightwave Technology (JLT)*, 2017

Aug 2016 Amirali Ghofrani, Miguel Angel Lastras-Montaño, **Yuayng Wang**, and Kwang-Ting Cheng. "In-place Repair for Resistive Memories Utilizing Complementary Resistive Switches". *International Symposium on Low Power Electronics and Design (ISLPED)*, San Diego, August 2016.

Apr 2016 Charles Hawkins, Jaume Segura, and Payman Zarkesh-Ha. "CMOS Digital Integrated Circuits: A First Course", (**Yuyang Wang**, and Yue Yin Trans.). *China Machine Press*, Beijing, China, April 2016. (Original work published by *SciTech Publishing*, New Jersey, 2013).

Mar 2015 Chao Xu, Felix Xiaozhu Lin, **Yuyang Wang**, and Lin Zhong. "Automated OS Level Device Runtime Power Management". *Proc. ACM Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2015.

May 2014 Sandip Kundu, and Aswin Sreedhar. "Nanoscale CMOS VLSI Circuits: Design for Manufacturability", (**Yuyang Wang**, and Wenao Xie Trans.). *Science Press*, Beijing, China, May 2014. (Original work published by *McGraw Hill*, New York, 2010).

Professional Skills

EDA Tools Cadence Virtuoso, Encounter, Synopsys Design Compiler, Optsim, Mentor Graphics Modelsim, Calibre, NI Multisim, EAGLE PCB Design, Advanced Design System (ADS), Xilinx ISE/Vivado.

Computing **SW/HW Programming Languages:** C, C++, Matlab, Verilog, VHDL, Verilog-A, System Verilog, HSPICE, MIPS Assembly.
Scripting Languages: Linux Shell Script (Bash), Cadence SKILL, Python.
Operating Systems: Windows, Linux and macOS.

Laboratory **Electronic:** Soldering, oscillloscope, network analyzer, etc.
Optical: Fiber handling, edge/vertical coupling, optical power meter, integrating sphere, etc.

Languages

Mandarin **Native language**

English **First foreign language** *Conversationally fluent*

Korean **Basic knowledge** *Simple daily sentences*

Honors and Scholarships

09.2015–12.2015 **ECE Department Fellowship**, *University of California*, Santa Barbara.

06.2015 **Outstanding Thesis Award of the Department**, *Tsinghua University*, Beijing, China.

10.2014 **Scholarship for Excellence in Sports**, *Tsinghua University*, Beijing, China.

Additional Activities

- Classical Piano
- Digital Photography
- Soccer