Yuyang Wang

Curriculum Vitae

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Educational Background

03.2018–Present **Ph.D. Candidate in Computer Engineering**, *University of California*, Santa Barbara, CA.
- Advisor: Prof. Kwang-Ting (Tim) Cheng.
- Research interest: Variation-aware modeling and optimization of silicon photonic interconnects and systems.

09.2015–03.2018 **M.S. in Computer Engineering**, *University of California*, Santa Barbara, CA, *GPA: 4.0/4.0*.
- Advisor: Prof. Kwang-Ting (Tim) Cheng.
- Selected courses: Advanced VLSI Design, Semiconductor Laser, Electronic and Photonic Integration and Packaging.

09.2011–07.2015 **B.Eng. in Electronic Engineering**, *Tsinghua University*, Beijing, China, *GPA: 88/100*.
- Thesis: *The Separation Scheme of Control and Traffic Coverage in Hyper-Cellular Network for LTE: Design and Implementation,* Outstanding Thesis Award of the Department.

09.2013–12.2013 **Non-Degree Exchange Program**, *Korea Advanced Institute of Science and Technology (KAIST)*, Daejeon, Korea, *GPA: 4.12/4.3*.

Internship

06.2018–09.2018 **Design Engineering Intern**, *Cadence Design Systems*, San Jose, CA.
- Supervisor: Dr. Gilles Lamant.
- Project: To be determined.

07.2014–09.2014 **Student Intern**, *Rice Efficient Computing Group (RECG), Rice University*, Houston, TX.
- Supervisor: Prof. Lin Zhong.
- Project: Automated OS Level Device Runtime Power Management.

Publication

Conference Paper

Nov 2018 **Yuyang Wang**, M. Ashkan Seyedi, Jared Hulme, Marco Fiorentino, Raymond G. Beausoleil, and Kwang-Ting Cheng. "Bidirectional Tuning of Microring-based Silicon Photonic Transceivers for Optimal Energy Efficiency". Submitted to *International Conference On Computer Aided Design (ICCAD)*, San Diego, U.S.A., 2018.

Mar 2018 **Yuyang Wang**, M. Ashkan Seyedi, Rui Wu, Jared Hulme, Marco Fiorentino, Raymond G. Beausoleil, and Kwang-Ting Cheng. "Energy-Efficient Channel Alignment of DWDM Silicon Photonic Transceivers". *Design, Automation and Test in Europe (DATE)*, Dresden, Germany, 2018.

Jan 2018 Rui Wu, M. Ashkan Seyedi, **Yuyang Wang**, Jared Hulme, Marco Fiorentino, Raymond G. Beausoleil, and Kwang-Ting Cheng. "Pairing of Microring-based Silicon Photonic Transceivers for Tuning Power Optimization". *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju, Korea, 2018.

Mar 2017 Rui Wu, **Yuyang Wang**, Zeyu Zhang, Chong Zhang, Clint L. Schow, John E. Bowers, and Kwang-Ting Cheng. "Compact Modeling and Circuit-Level Simulation of Silicon Nanophotonic Interconnects". *Design, Automation and Test in Europe (DATE)*, Lausanne, Switzerland, 2017.

Aug 2016 Amirali Ghofrani, Miguel A. Lastras-Montaño, **Yuayng Wang**, and Kwang-Ting Cheng. "In-place Repair for Resistive Memories Utilizing Complementary Resistive Switches". *International Symposium on Low Power Electronics and Design (ISLPED)*, San Diego, 2016.

Mar 2015 Chao Xu, Felix Xiaozhu Lin, **Yuyang Wang**, and Lin Zhong. "Automated OS Level Device Runtime Power Management". *Proc. ACM Int. Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2015.

Journal Paper

Jan 2017 Zeyu Zhang, Rui Wu, **Yuyang Wang**, Chong Zhang, Eric Stanton, Kwang-Ting Cheng, Clint L. Schow, and John E. Bowers. "Compact Modeling for Silicon Photonic Heterogeneously Integrated Circuits". Submitted to *Journal of Lightwave Technology (JLT)*, 2017

Book Translation

Apr 2016 Charles Hawkins, Jaume Segura, and Payman Zarkesh-Ha. "CMOS Digital Integrated Circuits: A First Course", (**Yuyang Wang**, and Yue Yin Trans.). *China Machine Press*, Beijing, China, 2016. (Original work published by *SciTech Publishing*, New Jersey, 2013).

May 2014 Sandip Kundu, and Aswin Sreedhar. "Nanoscale CMOS VLSI Circuits: Design for Manufacturability", (**Yuyang Wang**, and Wenao Xie Trans.). *Science Press*, Beijing, China, 2014. (Original work published by *McGraw Hill*, New York, 2010).

Posters and Talks

03.2018 **Optimal Pairing and Non-Uniform Channel Alignment of Microring-based Transceivers for Comb Laser-Driven DWDM Silicon Photonics**.
- Talk at the 2018 Optical/Photonic Interconnects for Computing Systems (OPTICS) workshop, Dresden, Germany.

01.2018 **Variation-Aware Modeling and Design of Silicon Photonic Systems**.
- Talk at the ECE Departmental Seminar, Hong Kong University of Science and Technology, Hong Kong.

03.2017 **Variation-Aware Modeling and Design of Nanophotonic Interconnects**.
- Poster at the 2017 Optical/Photonic Interconnects for Computing Systems (OPTICS) workshop, Lausanne, Switzerland.

Professional Skills

EDA Tools Cadence Virtuoso, Encounter, Synopsys Design Compiler, Optsim, Mentor Graphics Modelsim, Calibre, NI Multisim, Advanced Design System (ADS), Xilinx ISE/Vivado.

Computing **Programming Languages:** C, C++, MIPS Assembly.
Scripting Languages: Linux Shell Script (Bash), MATLAB, Python.
Hardware Discription Languages: Verilog, Verilog-A, HSPICE, VHDL.
Operating Systems: Windows, Linux and macOS.

Laboratory **Electronic:** Soldering, probe station, oscillloscope, network analyzer, etc.
Optical: Fiber handling, edge/vertical coupling, integrating sphere, etc.

Languages

Native **Mandarin Chinese**

First Foreign **English** *Conversationally fluent*

Others **Korean** *Simple daily sentences*

Honors and Scholarships

09.2015–12.2015 **ECE Department Fellowship**, *University of California*, Santa Barbara, CA.

06.2015 **Outstanding Thesis Award of the Department**, *Tsinghua University*, Beijing, China.

10.2014 **Scholarship for Excellence in Sports**, *Tsinghua University*, Beijing, China.

Additional Activities

- Classical Piano
- Digital Photography
- Soccer