

Ming GAO

ECE Department, University of California, Santa Barbara
Santa Barbara, CA 93106-9560, U. S. A.
Cell: 626-244-6080 Office: 805-893-5678
E-mail: mgao@ece.ucsb.edu URL: <http://cadlab.ece.ucsb.edu/~mgao>

OBJECTIVE

To obtain a full-time summer internship on verification, validation, and testing of System-on-a-Chip

EDUCATION

PhD in Computer Engr. **DEPT. OF ECE, UNIVERSITY OF CALIFORNIA, SANTA BARBARA, USA, 2006 - PRESENT**
Research Topic: Design for Resilience in Cost-sensitive SoCs
Research Advisor: Professor Kwang-Ting (Tim) Cheng
MS in Systems Engr. **SYSTEMS ENGINEERING INSTITUTE, XIAN JIAOTONG UNIVERSITY, CHINA, 2003 - 2006**
Research Interests: Network Security, SoC Design. (Exempt from entrance exam, Rank: 2/48)
Thesis Title: *Key Technology for High-Speed Network Intrusion Detection on SoPC*
BS in Information Engr. **DEPT. OF INFORMATION ENGR., XIAN JIAOTONG UNIVERSITY, CHINA, 1999 - 2003**
Study Emphasis: Telecommunication and Image Processing

RESEARCH INTERESTS

- Verification, Post-silicon Validation, Testing for SoC
- In-field and/or Online Testing and Self-Repair for SoC/NoC
- Cost-/Power-efficient Application/Domain Specific Computing

SELECT PUBLICATIONS

- **M. Gao** and K.T. Cheng, "Low Overhead Time-Multiplexed Online Checking: A Case Study of an H.264 Decoder," in Proceedings of the 18th Asian Test Symposium (ATS'09). IEEE Computer Society, Taichung, Taiwan. 2009.
- **M. Gao**, H.M. Chang, P. Lisherness, K.T. Cheng, "Time-Multiplexed Online Checking: A feasibility study," in Proceedings of the 17th Asian Test Symposium (ATS'08). IEEE Computer Society, Sapporo, Japan. 2008.
- **M. Gao**, K. Zhang, J. Lu, "Efficient Packet Matching for Gigabit Network Intrusion Detection using TCAMs," pp. 249-254, 20th International Conference on Advanced Information Networking and Applications (AINA'06), 2006.

RESEARCH PROJECTS

- **Time-Multiplexed Online Checking (TMOC) for Cost-Sensitive SoCs, UCSB 2007 - 2009**
Sponsor: Resilient Theme, Gigascale Systems Research Center (GSRC, www.gigascale.org)
Keywords: Online Testing, Error Detection, Reconfigurable Checker.
Tools: Xilinx ISE, XPS, XSG; Matlab, Simulink; ModelSim; SoC Encounter; Design Compiler; Certify, Synplify Pro.
Motivation: Reduce online checking overhead and improve product in-field availability for cost-sensitive SoCs.
Methodology: Multiple sub-systems temporarily share one reconfigurable checker space.
Demo: An FPGA demo using TV-to-VGA decoder on Xilinx XUP system: <http://cadlab.ece.ucsb.edu/~mgao/tmoc>
- **NetFPGA Case Study: A P2P Traffic Monitor for Multi-Gigabit Router, Xilinx China, Summer 2008**
Motivation: Demonstrate the efficiency of NetFPGA to Asian networking research community.
Methodology: A header-and-payload matching based P2P flow identifier with firewall in a gigabit router inside NetFPGA.
Demo: I lead a workshop for NetFPGA user community in Xilinx Shanghai. http://www.openhw.org/project/view_240.html
- **Signature Matching Offload Engine for High Speed Network Intrusion Detection, XJTU 2004 - 2006**
Sponsor: China Hi-Tech Research and Development Program ("863" Program)
Keywords: High Speed Networking, Intrusion Detection, Pattern Recognition;
Tools: Xilinx ISE, EDK; Synplify Pro; ModelSim; libSVM; Visual Studio.
Motivation: Leverage XJTU-IDS system for Gigabit links using application specific hardware architectures.
Methodology: NIDS signature matching hardware engine using proposed cascaded TCAM architecture.
Demo: An NIDS FPGA prototype system on Xilinx ML310 evaluation board.