ChiYun Compact: A Novel Test Compaction Technique for Responses with Unknown Values

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Abstract

This paper proposes a response compactor, named ChiYun compactor, to compact scan-out responses in the presence of unknown values. By adding storage elements into an Xor network, a ChiYun compactor can offer multiple chances for a scan-out response to be observed at ATE channels in one to several scan-shift cycles. We also develop a mathematical analysis to predict the percentage of scan-out responses masked by the unknown values for the ChiYun compactor. With this analysis, we can derive the optimal configuration of a ChiYun compactor for minimizing the masking of scan-out responses. We further propose a selection scheme for the ChiYun compactor to selectively observe partial Xor results for improving the fault coverage. The experimental results demonstrate the effectiveness of the proposed mathematical analysis and the selection scheme. We also demonstrate that the unknown tolerance of a ChiYun compactor is higher than that of a state-of-the-art response compactor proposed in [11].

1. Introduction

To reduce test data volume and test application time, researchers have recently shown increasing interest in the areas of input stimulus compression and output response compaction. For input compression, the goal is to use a limited number of ATE channels to supply the scan-in tests for all scan chains. Thus, input compression requires an on-chip mechanism to de-compress the tests from ATE channels before applying them to the scan chains. This input compression can be achieved by taking advantage of the ”don’t cares” in the test cubes. Several methods for this input compression problem have been proposed by using coding strategies [1], BIST test sequences [2], or linear expansion [3].

On the other hand, the goal of output response compaction is to generate a ”signature” for the scan-out responses so that the signature can be observed through a limited number of ATE channels and be compared with the good-circuit signature. Thus, a lossless compression for the scan-out responses is not absolutely necessary as long as the faulty-circuit signature remains differentiable from the good-circuit signature.

The key barrier to effective output response compaction is the presence of unknown values (or unknowns) when computing the good-circuit responses. If no unknown value exists, a *time compactor*, such as MISRs (Multiple Input Signature Registers), can compress an infinitely long output sequence into a fixed-length signature and guarantee a negligible aliasing probability. The method proposed in [4] applies the concept of MISR for scan-out response compaction. However, just one unknown in the scan-out responses would result in an unpredictable good-circuit signature and, thus, no faulty-circuit signature can be differentiated from it. The methods proposed in [5] and [6] attempt to mask unknowns before they are fed to a time compactor. The method in [5] requires a pattern-dependent circuitry and the one in [6] requires a special ATPG to support its compaction scheme.

The *selective compactors* proposed in [7] and [8] select a small subset of data from the scan chains for observation on the ATE channels. Based on the fault simulation results with respect to the target fault model, the compactor selects only those scan-out responses containing a faulty value for observation. All other responses are discarded. However, an important assumption of structural testing is that the patterns for the target modeled faults often detect many un-modeled faults as well. Therefore, discarding a majority of scan-out responses would likely degrade the overall test quality. The method proposed in [9] also chooses few scan chains to either observe or block. One limitation of these methods [7] [8] [9] is the requirement of a customized ATPG to support their selective compaction scheme.

Another class of response compactors, called *spatial compactors*, allow unknown values propagating to outputs and still can observe majority of the scan-out responses. The method proposed in [10] uses XOR networks to build a spatial compactor. The methods proposed in [11] and [12] use storage elements along with XOR networks to further improve the compaction ratio and unknown tolerance for a spatial compactor. These methods [10], [11], and [12] all guarantee that no single error value would be masked by a single unknown value. For the case that multiple unknown values are present among responses, different configurations of a compactor in [10], [11], and [12] would result in different probabilities of a response being masked by unknowns. However, no analytical method was proposed in [10], [11], and [12] to predict this masking probability. Hence the optimal configuration of a compactor with respect to the masking probability cannot be derived systematically.

In this paper, a novel technique is proposed to construct a spatial compactor, called *ChiYun compactor*. With some storage elements added into the compactor, a scan-out response has multiple chances to be observed on different ATE channels in one to several scan-shift cycles. A ChiYun compactor can also guarantee that no single error value would be masked by a single unknown value. We propose an efficient analytical method for ChiYun compactors to predict the probability that a scan-out response is masked by the unknowns. With this analytical method, we can derive the optimal configuration of a ChiYun compactor to maximize the probability of observing a scan-out response in the presence of unknowns. In addition, a selection scheme is also proposed for a ChiYun compactor to selectively observe the Xor results containing faulty values and hence improve the fault coverage. This selection scheme does not require a pattern-dependent circuitry (as [5]) nor a customized ATPG (as [6] [7] [8] [9]). With a given test set and a fault model, the proposed algorithm for selection signal generation can maximize the observation of the fault effects for the modeled faults. The experimental results show that a ChiYun compactor achieves a lower masking probability of scan-out responses in the presence of unknowns than that of a Block compactor ([11]) does. The experimental results also show that the proposed selection scheme can effectively improve the fault coverage.

2. Test Response Compaction with Xor Gates

To build a compaction scheme on scan-out responses, error detection on the compacted response signatures is the first concern. The definition of an *error value* (or *error*) is an scan-out response with a value different from its good-circuit response. If there is an error among scan-out responses, we hope this error can make the output signature different from the good-circuit signature and hence this faulty circuit can be identified. When Xor gates are used for response compaction and even number of errors arrive at an Xor tree in the same scan-shift cycle (as shown in Figure 1(a)), these even number of errors would cancel one another and the output result would be as same as the good-circuit result.

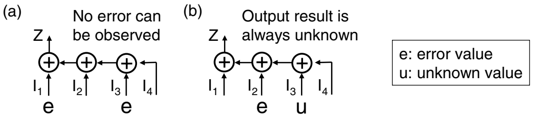


Figure 1: Masking effect with an Xor tree.

Furthermore, we may lose more on error detection when *unknown values* (or *unknowns*) appear in the good-circuit responses. The definition of an unknown is a scan-out response whose good-circuit value cannot be determined by simulation. Once an unknown arrives at an Xor tree, the good-circuit output value of this Xor tree would become unknown. With an unknown good-circuit response, no comparison can be made to identify a faulty Xor result. As shown in Figure 1(b), an unknown on I_3 makes the output result of this Xor tree undetermined. Therefore, even an error is on I_1, I_2, or I_4, the error cannot be detected on the Xor tree's output.

In the following two sections, we will emphasize more on the impact of the unknown-induced masking on the ChiYun compactor and show how to design a ChiYun compactor to minimize the unknown-induced masking. We will also show how a ChiYun compactor can avoid even-error masking.

3. R-type ChiYun Compactor

3.1. Basic Idea of a ChiYun Compactor

Figure 2 shows an exemplary ChiYun compactor with eight inputs (I_1-I_8) and 2 external outputs (Z_1-Z_2). Each input (I_1-I_8) connects to a scan chain (chain1-chain8) and each external output connects to a tester channel. This exemplary ChiYun compactor is composed of Xor sub-arrays and memory elements. For each scan chain, a 2x3 Xor sub-array and 2 memory elements are constructed to propagate a response into different external outputs in different scan-shift cycles. For the size of an Xor sub-array, the number of rows is equal to the number of external outputs; and the number of columns is one more than the number of memory elements used in each sub-array. In each Xor sub-array, the input of its first column is the current response of the scan-chain output; the inputs of its second and third column are the one-cycle-earlier response and two-cycle-earlier response of the same scan-chain output. For each column, one Xor gate is used to propagate the input response to an external output. The *i*th row of an Xor sub-array is connected to the *i*th row of all other sub-arrays through Xor gates, and this Xor result will propagate to the corresponding external output (Z_i).

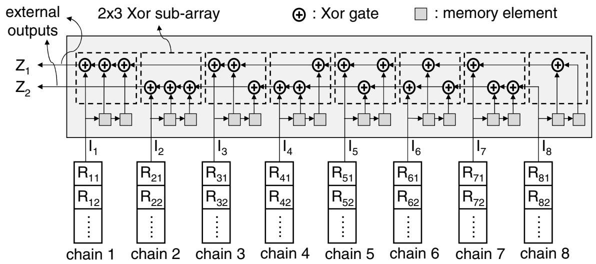
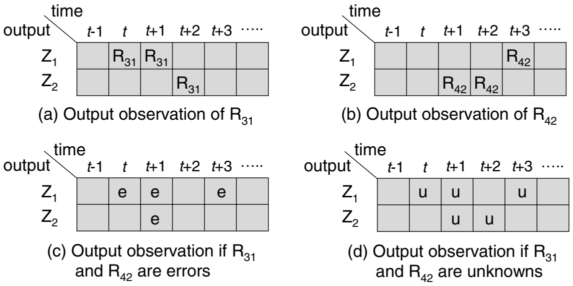


Figure 2: Example of a 8-to-2 ChiYun compactor.

When a scan-out response arrives at an input of a ChiYun compactor, this response will be stored in memory elements and hence can be observed at external outputs in multiple scan-shift cycles. Figure 3(a) and (b) show two examples of how a response can be observed at the external outputs of the exemplary ChiYun compactor in Figure 2. R_{ij} represents the response in the jth scan cell of ith scan chain (Figure 2). As shown in Figure 3(a), response R_{31} arrives at the compactor input I_3 in scan-shift cycle t and will be propagated to external outputs through the corresponding Xor sub-array of chain3. In scan-shift cycle t, R_{31} is the input to the first column of the Xor sub-array and hence is observed by Z_1. In scan-shift cycle $t+1$, R_{31} moves to the memory element right next to I_3 and is observed at Z_1. In scan-shift cycle $t+2$, R_{31} moves to the right-most memory element of the I_3 sub-array and is observed at Z_2. Similarly, R_{42} arrives at the compactor in scan-shift cycle $t+1$ and will be observed at outputs in scan-shift cycles $t+1$ to $t+3$ as shown in Figure 3(b).



output \ time	t-1	t	t+1	t+2	t+3	·····
Z_1		R_{31}	R_{31}			
Z_2				R_{31}		

(a) Output observation of R_{31}

output \ time	t-1	t	t+1	t+2	t+3	·····
Z_1					R_{42}	
Z_2			R_{42}	R_{42}		

(b) Output observation of R_{42}

output \ time	t-1	t	t+1	t+2	t+3	·····
Z_1		e	e		e	
Z_2			e			

(c) Output observation if R_{31} and R_{42} are errors

output \ time	t-1	t	t+1	t+2	t+3	·····
Z_1		u	u		u	
Z_2			u	u		

(d) Output observation if R_{31} and R_{42} are unknowns

Figure 3: Example of propagating responses in a ChiYun compactor.

Figure 3(c) and (d) show how error values and unknown values could interact with one another. If R_{31} and R_{42} are both error values, two error values will cancel each other at Z_2 in scan-shift cycle $t+2$, and the external outputs will observe 4 error values as shown in Figure 3(c). If R_{31} and R_{42} are both unknown values, the external outputs will observe 5 unknown values as shown in Figure 3(d). With the distribution of unknown values in Figure 3(d), some responses (other than R_{31} and R_{42}) may not be observed at any external output in any scan-shift cycle. For example, R_{71} and R_{52} are propagated to an external output which observes an unknown value for the three consecutive cycles, and hence these two responses cannot be observed in any of these cycles.

Figure 4 represents the Xor sub-arrays by binary matrices, where 1 at element (i, j) in the matrix means the input of jth column will be propagated to the ith external output through an Xor gate.

$$\begin{array}{cccccccc} \begin{pmatrix}1&1&1\\0&0&0\end{pmatrix} & \begin{pmatrix}0&0&0\\1&1&1\end{pmatrix} & \begin{pmatrix}1&1&0\\0&0&1\end{pmatrix} & \begin{pmatrix}0&0&1\\1&1&0\end{pmatrix} & \begin{pmatrix}1&0&1\\0&1&0\end{pmatrix} & \begin{pmatrix}0&1&0\\1&0&1\end{pmatrix} & \begin{pmatrix}1&0&0\\0&1&1\end{pmatrix} & \begin{pmatrix}0&1&1\\1&0&0\end{pmatrix} \\ \text{chain 1} & \text{chain 2} & \text{chain 3} & \text{chain 4} & \text{chain 5} & \text{chain 6} & \text{chain 7} & \text{chain 8} \end{array}$$

Figure 4: Binary matrices for Xor sub-arrays of each scan chain.

3.2. General Property of a R-type ChiYun Compactor

The key to construct a ChiYun compactor is to construct the Xor matrix for each scan chain. For a Z x C matrix, Z is the number of external outputs in use and C is the number of input responses for each Xor sub-array. For example, $Z = 2$ and $C = 3$ in Figure 4. For a Regular-type (R-type) ChiYun compactor, each Xor matrix has the same number of Xor gates in each column. The number of Xor gates in each column is denoted as W_R. If no two matrices are identical, then a R-type ChiYun compactor can guarantee that no two errors among the scan-out responses will cancel each other out and no single error will be masked by a single unknown. To satisfy the above condition, the maximum number of scan chains (N_{max}) that a R-type ChiYun compactor can support is:

$$N_{max} = \binom{Z}{W_R}^C \tag{1}$$

where $\binom{i}{j}$ means the possible combinations of choosing j items from i items.

Table 1 compares the maximum numbers of supported scan chains of ChiYun compactors, Block compactor [11], and X-Compact [10]. For a ChiYun compactor, we set the number of matrix columns (C) to be 4 and the number of Xor gates per column (W_R) to be 1. For a Block compactor, we set the block size as same as C of a ChiYun compactor (4) and the number of Xor gates per column to be 3, which is larger than that of a ChiYun compactor. For X-Compact, we report the maximum number of supported scan chains with the given outputs. As shown in the Table, a R-type ChiYun compactor always supports more scan chains than a Block compactor or an X-Compactor which uses the same number of external outputs. It implies that ChiYun compactors can achieve a higher compaction ratio (defined as the number of supported scan chains divided by the number of external outputs).

# of output	2	3	4	5	6	7
R-type ChiYun ($C = 4, W_R = 1$)	16	81	256	625	1296	2401
Block (block size=4,$W = 3$)	14	55	140	285	506	20
X-Compact	2	3	4	10	20	35

Table 1: maximum number of supported scan chains of R-type ChiYun compactor, Block compactor, and X-Compact.

3.3. Unknown Tolerance of R-type ChiYun Compactors

To identify which scan-out responses would be masked by unknowns, we first map the unknowns among scan-out responses to a *timing table* as shown in Figure 3. A *tile* in a timing table represents the value at an output in a scan-shift cycle. After mapping unknowns to the timing table, this timing table can indicate which output in which scan-shift cycle will observe an unknown. Based on the mapped tiles of these unknowns, we can find out which response cannot be observed by checking its corresponding mapped tiles in the timing table, such as responses R_{71} and R_{52} in Figure 3(d).

For a R-type ChiYun compactor, given the number of external outputs (Z) and the number of 1's per column (W_R), increasing the number of columns (C) in the Xor matrices can provide more scan-shift cycles for a response to be observed at external outputs. However, in this case, an unknown will also have more chances to propagate to external outputs. Therefore increasing C would also increase the probability that an external output observes an unknown in each scan-shift cycle.

Table 2 shows how different configurations of the matrix in a R-type ChiYun compactor can affect the probability of a response being masked by unknowns and thus unobservable. In this experiment, we set $Z = 10$ and $W_R = 1$ to build the Xor matrices for 1000 scan chains. 0.1 % of the output responses are randomly generated as unknowns. As the results shown, the percentage of unobservable responses does not always improve when using a larger C. The unobservable percentage hits the lowest when $C = 4$.

# of columns	$C = 3$	$C = 4$	$C = 5$	$C = 6$	$C = 7$
unobservable %	2.43	1.96	2.10	2.78	3.16

Table 2: Percentage of unobservable responses by given 10 outputs, 1000 scan chain, and 0.1% unknown.

To further reduce the probability of a response being masked by unknowns, we hope that the number of Xor gates in a matrix does not necessarily goes up when the number of its columns increases. In the next section, we introduce another type of ChiYun compactors, named Flexible-type (F-type) ChiYun compactors, to achieve this purpose.

4. F-type ChiYun Compactors

4.1. General Property of a F-type ChiYun Compactor

The difference between a R-type ChiYun compactor and a F-type ChiYun compactor is the way to construct their Xor sub-arrays. Figure 5 shows one possible combination of Xor matrices for a 8-to-2 F-type ChiYun compactor. In a F-type ChiYun compactor, the total number of 1's in an Xor matrix is fixed, but the number of 1's in each column could be different. Hence, the total number of 1's in an Xor matrix is no longer a multiple of the number of columns (as for a R-type ChiYun compactor). We can select a proper number of 1's in an Xor matrix to minimize the unknown-induced masking.

$$\begin{array}{cccccccc} \begin{pmatrix}1&1&0\\0&0&0\end{pmatrix} & \begin{pmatrix}0&0&0\\1&0&1\end{pmatrix} & \begin{pmatrix}0&1&0\\0&0&1\end{pmatrix} & \begin{pmatrix}0&0&1\\0&0&1\end{pmatrix} & \begin{pmatrix}1&0&0\\0&0&1\end{pmatrix} & \begin{pmatrix}0&0&1\\0&1&0\end{pmatrix} & \begin{pmatrix}1&0&1\\0&0&0\end{pmatrix} & \begin{pmatrix}0&0&0\\1&1&0\end{pmatrix} \\ \text{chain 1} & \text{chain 2} & \text{chain 3} & \text{chain 4} & \text{chain 5} & \text{chain 6} & \text{chain 7} & \text{chain 8} \end{array}$$

Figure 5: Binary matrices for a F-type ChiYun compactor.

The other rule for a F-type ChiYun compactor is that no Xor matrix can be a horizontally-shifted version of another matrix. Figure 6 shows an example of how a horizontally-shifted version of an Xor matrix can affect the original Xor matrix. In Figure 6, matrix M_2 is a one-column right-shifted version of matrix M_1. If a response R_{21} arrives at the Xor sub-array of M_2 in scan-shift cycle t and another response R_{12} arrives at the Xor sub-array of M_1 in scan-shift cycle $t + 1$, these two responses will be mapped to the same two tiles in the timing table, (Z_1, $t + 1$) and (Z_1, $t + 2$). It implies that if R_{21} and R_{12} are both errors, then they would mask each other. If one of them is an unknown, then the other response will become unobservable.

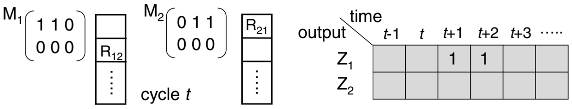


Figure 6: Horizontally-shifted version of an Xor matrix for a F-type ChiYun compactor.

With the above two rules, a F-type ChiYun compactor can guarantee that no two errors can mask each other and no single error will be masked by a single unknown. If the number of 1's in a matrix (denoted as W_F) is odd, then no odd number of errors can be masked.

Given the number of outputs Z, the number of columns C, and the number of 1's in a matrix W_F, the maximum number of supported scan chains N_{max} for a F-type ChiYun compactor would be:

$$N_{max} \quad = \quad \sum_{i=1}^{min(Z,W_F)} \binom{Z}{i}\binom{Z \cdot C - C}{W_F - i} \qquad (2)$$

Table 3 lists the maximum number of supported scan chains of F-type compactors and R-type ChiYun compactors. We use the same parameters as those used in Table 3 ($W_R = 1$ and $C = 4$) for the R-type compactors and the use the same total number of 1's in an Xor matrix for the F-type compactors ($W_F = 4$). The reported numbers show that a F-type ChiYun compactor can support more scan chains than a R-type ChiYun compactor does for any number of external outputs in use.

# of output	2	3	4	5	6	7
R-type	16	61	256	625	1296	2401
F-type	69	425	1325	3025	5781	9849

Table 3: Maximum number of supported scan chains of F-type and R-type ChiYun compactors. $C = 4$, $W_R = 1$, and $W_F = 4$.

Given the numbers of scan chains (N_{SC}), matrix columns (C), and 1's in an Xor matrix (W_F), the following equations show the numbers of required memory elements (N_{FF}) and Xor gates (N_{Xor}) for a F-type ChiYun compactor.

$$N_{FF} \quad = \quad (C-1) \cdot N_{SC} \qquad (3)$$

$$N_{Xor} \quad = \quad W_F \cdot N_{SC} \qquad (4)$$

4.2. Unknown Tolerance of F-type ChiYun Compactors

With a different number of matrix columns (C) and a different number of 1's in each matrix (W_F), the unknown tolerance of a ChiYun compactor could be different. Table 4 shows the percentages of unobservable responses with different C's but fixed W_F. The results indicate increasing C always reduces the unobservable percentage.

C	3	4	5	6	10	20
unobs. %	2.19	1.84	1.64	1.53	1.31	1.16

Table 4: Percentage of unobservable responses for different C with $Z = 10$, $W_F = 5$, 0.1% unknown, and 1000 scan chains.

Table 5 shows the percentage of unobservable responses with different W_F's but fixed C. As the results shown, increasing W_F may not always help the unobservable percentage. The lowest unobservable percentage is achieved when $W_F = 4$.

W_F	3	4	5	6	7
unobs. %	2.35	2.10	2.19	2.48	2.94

Table 5: Percentage of unobservable responses for different W_F with $Z = 10$, $C = 3$, 0.1% unknown, and 1000 scan chains.

The values of W_F and C affect not only the unknown tolerance but also the hardware overhead for a ChiYun compactor. In order to efficiently find the optimal values of W_F and C for a ChiYun compactor, we derive a mathematical equation to predict the percentage of unobservable responses. The parameters for calculating the percentage of unobservable responses include the number of scan chains (N_{SC}), the number of outputs (Z), the number of columns in each matrix C, the number of 1's in each matrix (W_F), and the probability that a scan-out response is an unknown (p). The percentage of unobservable responses (UP) is: (the long mathematical derivation is omitted here)

$$UP \quad = \quad \sum_{j=0}^{W_F} (-1)^j \cdot \binom{W_F}{j} \cdot \left(p \cdot \frac{\binom{Z \cdot C - j}{W_F}}{\binom{Z \cdot C}{W_F}} + 1 - p\right)^{C \cdot N_{SC}} \qquad (5)$$

Table 6 shows the predicted unobservable percentages obtained by Equation(5). We use the same parameters as those in Table 5. The "*" symbol in the table indicates the lowest unobservable percentage for the simulation result or the predicted result. As shown in the table, both simulation and prediction indicate that $W_F = 4$ would generate the lowest unobservable percentage for the given parameters. Although the predicted results do not precisely match the numbers derived by simulation, their difference is small and, most importantly, the predicted results can accurately identify the optimal configuration of a F-type ChiYun compactor.

W_F	3	4	5	6	7
simulation %	2.35	2.10*	2.19	2.48	2.94
predicted %	2.61	2.44*	2.67	3.19	3.97

Table 6: Unobservable percentage for different W_F with $Z = 10$, $C = 3$, $p = 0.1$, $N_{SC} = 1000$.

In Table 7, we further show the predicted unobservable percentages for different C's and compare the predicted results with the simulation results. Again, the predicted results can be used to identify the optimal number of W_F except one case. The only exception is for $C = 5$. In this case, the predicted results for $W_F = 4$ and $W_F = 5$ are almost the same and the difference of their simulation results is relatively small.

C	W_F	3	4	5	6	7
3	simulation %	2.35	2.10*	2.19	2.48	2.94
	predicted %	2.61	2.44*	2.67	3.19	3.97
4	simulation %	2.21	1.84*	1.86	1.99	2.33
	predicted %	2.39	2.11*	2.19	2.51	3.03
5	simulation %	2.13	1.72	1.64*	1.73	1.96
	predicted %	2.26	1.91*	1.92	2.14	2.52
6	simulation %	2.07	1.64	1.53*	1.58	1.78
	predicted %	2.17	1.79	1.75*	1.90	2.20

Table 7: Unobservable percentage for different W_F and C with $Z = 10$, $p = 0.1$, $N_{SC} = 1000$.

Several other parameters, such as the number of external outputs (Z), the number of scan chains (N_{SC}), and the percentage of unknown responses (p), may also affect the unobservable percentage and, thus, result in different optimal W_F's. Table 8 shows the predicted and simulation results for several different combinations of parameters.

parameters	W_F	3	4	5	6	7
$Z = 10, N_{SC} = 500$	simulation %	15.66*	17.71	20.91	25.30	30.34
$C = 4, p = 0.005$	predicted %	16.03*	18.41	22.21	27.04	32.60
$Z = 10, N_{SC} = 500$	simulation %	0.562	0.418	0.371*	0.379	0.409
$C = 5, p = 0.001$	predicted %	0.595	0.445	0.421*	0.460	0.549
$Z = 5, N_{SC} = 250$	simulation %	0.647	0.614*	0.677	0.870	1.043
$C = 3, p = 0.001$	predicted %	0.961	0.934*	1.118	1.489	2.085
$Z = 5, N_{SC} = 250$	simulation %	0.448	0.364	0.312*	0.318	0.347
$C = 6, p = 0.001$	predicted %	0.595	0.445	0.421*	0.460	0.549

Table 8: Unobservable percentage for different W_F, C, Z, p, and N_{SC}.

4.3. Comparison with Block Compactors

We further performed experiments on two industrial designs to compare the unobservable percentage and the fault coverage between a F-type ChiYun compactor and Block compactor [11]. Table 9 shows the number of scan flip-flops, the gate count, the number of test patterns, and the number of *ATPG-detected faults*. The test patterns are compressed stuck-at-fault patterns generated by an industrial ATPG system. The numbers of test patterns before compression are 3063 and 25859 for designs D1 and D2, respectively.

Circuit	# of scan FFs	Gate Count	# of test pttn	ATPG det flt
D1	4990	722K	542	985234
D2	65560	870K	1514	1835582

Table 9: Circuit information for two industrial designs.

In this experiment, the unknown values are randomly generated among scan-out responses according to a given unknown probability p. For a fair comparison, the block size of the Block compactor is set to be the same as the number of columns C in the ChiYun compactor. For both compactors, we report the best result among several different numbers of Xor gates (as W_F in a ChiYun compactor). Table 10 and 11 show the results of different combinations of parameters for designs D1 and D2, respectively. The first three columns in Table 10 and 11 list the parameters used for each compactor. Column 4 shows the compaction ratio of the compactors. Columns 5 and 6 compare the unobservable percentages of the two compactors. Columns 7 and 8 compare the number of undetected faults. The results show that, for every combination of parameters, the ChiYun compactor always achieves a lower unobservable percentage than the corresponding Block compactor. Also, the ChiYun compactor can have less number of undetected faults for all combinations of parameters except one case.

5. Fault Coverage Improvement with a Selection Scheme

5.1. Basic Idea of the Selection Scheme

In this section, we propose a selection scheme to selectively observe some responses containing faulty values while using a ChiYun compactor. An algorithm of generating control signals for this selection scheme is also proposed to optimize the fault coverage.

Figure 7 shows the design of a ChiYun compactor with the proposed selection scheme. This ChiYun compactor is modified from the exemplary ChiYun compactor in Figure 2. The external outputs Z_1 and Z_2 here receive the same results as those in the ChiYun compactor in Figure 2. The first difference of this modified ChiYun compactor is the connection among the Xor sub-arrays. Instead of connecting the ith row in an Xor sub-array directly to the ith row of the left-next Xor sub-array, we divide the entire Xor network into 8 *segments*. Each segment S_{ij} collects part of the Xor result in the ith row. The output Z_i observes the Xor results of all segments in the ith row. The second difference is that one extra external output Z_S and one extra control signal Sel are used in this selection scheme. By specifying the signal Sel, output Z_S can directly observe the Xor result on a targeted segment. If we select to observe the Xor result from segment S_{ij}, the observed result will be independent of the other segments.

parameters ($Z = 5$)			compaction	unobservable %		undet. flt	
N_{SC}	C	p	ratio	ChiYun	Block	ChiYun	Block
250	3	0.001	50X	0.61	0.81	35	61
250	5	0.003	50X	5.38	5.86	253	285
500	4	0.001	100X	2.15	2.21	156	144
500	5	0.003	100X	19.84	25.22	1258	1799

Table 10: Comparison on design D1.

parameters ($Z = 10$)			compaction	unobservable %		undet. flt	
N_{SC}	C	p	ratio	ChiYun	Block	ChiYun	Block
500	3	0.001	50X	0.37	0.55	77	170
500	5	0.003	50X	5.27	5.88	1900	2266
500	4	0.005	50X	15.66	16.15	6563	6978
1000	5	0.001	100X	1.64	2.34	553	887

Table 11: Comparison on design D2.

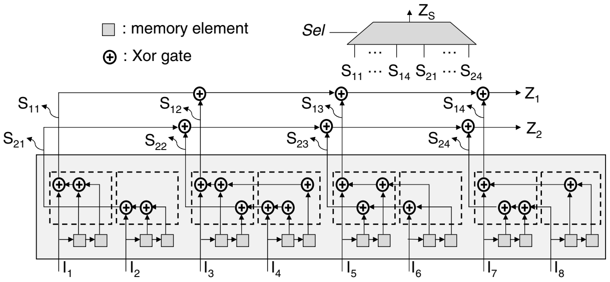
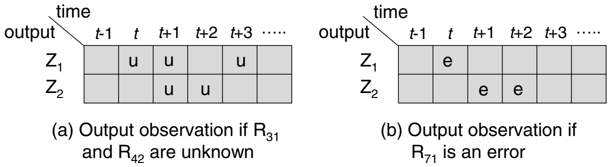


Figure 7: Selection scheme for a ChiYun compactor.

When an error propagates to an output Z_i, the error might be masked by an unknown in the ith row. However, this error may be detectable by direct observation of its corresponding segment, through Z_S, if no unknown is in this segment. For example, Figure 8(a) shows the timing table when both R_{31} and R_{42} are unknowns. If R_{71} is an error (as shown in Figure 8(b)), then this error cannot be observed at neither Z_1 nor Z_2 during scan-shift cycles t to $t+2$. With the selection scheme, if segment S_{24} is selected in scan-shift cycle t, this error can be observed at output Z_S in scan-shift cycle t. For a ChiYun compactor, an error could propagate to an output in multiple scan-shift cycles. So this selection scheme offers multiple chances to directly observe an originally-masked error at the output Z_S.



output \ time	t-1	t	t+1	t+2	t+3	·····
Z_1		u	u		u	
Z_2			u	u		

(a) Output observation if R_{31} and R_{42} are unknown

output \ time	t-1	t	t+1	t+2	t+3	·····
Z_1		e				
Z_2			e	e		

(b) Output observation if R_{71} is an error

Figure 8: Example of the selection scheme.

5.2. Algorithm for Selection Signal Generation

An important property of this selection scheme is that no matter how we select a segment to observe at output Z_S, the result observed at the original outputs (Z_1-Z_2 in Figure 7) remains the same. Therefore, most of the ATPG-detected faults are already detected by the original ChiYun compactor without this selection scheme. To consider which segments to observe at output Z_S, we only need to focus on the faults which cannot be detected by the original ChiYun compactor. Those faults are denoted as *compaction-undetected faults*.

The proposed algorithm for the selection signal generation consists of two stages. The first stage is to identify the compaction-undetected faults. The second stage is to specify the value at signal *Sel* to detect those compaction-undetected faults. The objective of this algorithm is to detect as many compaction-undetected faults as possible.

In the first stage, fault simulation, based on the original ChiYun compactor, is performed to identify the compaction-undetected faults. For each compaction-undetected fault, we also record how many times that the fault effects appear in the scan cells (i.e. the responses in the scan cells are erroneous) but those responses are all masked by unknowns. This count is denoted as *masked_count*.

In the second stage, another fault simulation run is performed only for those compaction-undetected faults. For each scan-shift cycle of each pattern, a value is specified at *Sel* trying to observe errors of those compaction-undetected faults at Z_S. If an error of a compaction-undetected fault is observed at Z_S, the fault is then dropped from the fault list; If a compaction-undetected fault produces erroneous scan-out responses but none of those erroneous responses can be observed by the specified value at *Sel*, the *masked_count* of that fault is then decreased by 1. When *masked_count* $= 1$, it means that this compaction-undetected fault cannot be detected by any future assignment of the *Sel* value if we miss this last chance when this fault produces erroneous scan-out responses. Therefore, for a compaction-undetected fault with *masked_count* $= 1$, we denote it as an *urgent fault*; for a fault with *masked_count* > 1, we denote it as a *non-urgent fault*. When we determine the value at *Sel*, our first goal is to detect as many urgent faults as possible. If several values at *Sel* can detect the same maximal number of urgent faults, our second goal is to detect as many non-urgent faults as possible.

5.3. Experimental Results for Selection Scheme

Table 12 and 13 show the results of applying this selection scheme for the two industrial designs D1 and D2. In this experiment, the selection scheme is applied to the same ChiYun compactors and test patterns used in Table 10 and 11. The numbers of segments used in the selection scheme are 16 and 32 for D1 and D2, respectively. In Table 12 and 13, the first three columns list the parameters used for each compactor. Column 4 and Column 5 list the numbers of undetected faults without and with using the selection scheme, respectively. Column 6 lists the improvement on the number of the undetected faults by applying the selection scheme. As the result shows, applying the selection scheme can detect most of the originally-undetected faults, 87.2% for D1 and 96.6% for D2 in average. The results demonstrate that the selection scheme indeed significantly reduce the fault coverage loss caused by the output compactor.

This fault coverage improvement does not come for free. One extra external output and several control bits for selection signal *Sel* are needed. For example, if 32 segments are used in the selection scheme, 5 bits are required for the selection signal *Sel*. Fortunately, the value at signal *Sel* needs not to be specified in every scan-shift cycle. For the scan-shift cycles in which no specific value at *Sel* is required, the value at *Sel* is a "don't care". Therefore, the control data for signal *Sel* can be further compressed through input compression scheme. Column 7 in Table 12 and 13 lists the percentages of the scan-shift cycles in which a specified value at *Sel* is required. As the results show, the overhead of control data required for the selection scheme is limited. Column 8 in Table 12 and 13 lists the runtime of the proposed algorithm for the selection scheme. The reported runtime shows that the proposed algorithm for selection signal generation is scalable to large designs.

parameters ($Z = 5$)			without selection	with selection (16 segments)			
N_{SC}	C	p	undet. flt	undet. flt	undet. flt improve %	specified %	runtime (sec)
250	3	0.001	35	4	88.6	0.02	830
250	5	0.003	253	14	94.9	1.63	815
500	4	0.001	156	34	78.2	1.43	812
500	5	0.003	1258	164	87.0	14.21	836
average					87.2	4.32	

Table 12: Results of selection scheme on design D1.

parameters ($Z = 10$)			without selection	with selection (32 segments)			
N_{SC}	C	p	undet. flt	undet. flt	undet. flt improve %	specified %	runtime (sec)
500	3	0.001	77	0	100.0	0.04	5592
500	5	0.003	1900	76	96.0	0.80	6166
500	4	0.005	6563	479	92.7	2.62	6313
1000	5	0.001	533	13	97.6	0.49	5301
average					96.6	0.99	

Table 13: Results of selection scheme on design D2.

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