

Digitally-Assisted Analog/RF Testing for Mixed-Signal SoCs

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Abstract

We propose a testing methodology for analog and radio-frequency (RF) circuitry that incorporates digital circuits for performance calibration and adaptation. We explore the reuse of built-in digital calibration circuitry, along with minor digital design-for-testability (DfT) modifications, to test and characterize analog/RF circuit performance. By observing the digital tuning signals captured in the digital calibration circuitry, the analog/RF performance can be closely estimated, thus enabling cost-effective Go/No-Go production testing. In this paper, we illustrate this testing methodology using a case study of a digitally-calibrated Weaver image-reject receiver.

Keywords – self-tuning circuit, digital calibration, analog testing, mixed-signal testing, RF testing

1. Introduction

Testing accounts for a significant portion of an integrated circuit's cost. Testing analog, mixed-signal and radio-frequency (RF) circuits is particularly costly due to the sophisticated test equipment required, the complex test settings, and lengthy testing time needed to obtain time and frequency-domain measurements [1]. Adding on-chip measurement circuitry either for built-in-self-test (BIST) or for facilitating automatic test equipment (ATE) measurements provides a mean to observe internal analog signals for performance measurement and reduces the overall testing cost. There have been a number of solutions provided for analog/mixed-signal [2] [3] as well as RF [4] transceivers circuits. These either require adding circuitry to the sensitive analog path or else are useful only for measuring limited specifications.

Digitally-assisted analog design [5] provides a potential opportunity for estimating the analog performance based on the digital domain data. Instances of this concept have been briefly discussed in some recent articles. In [6], for example, the calibration circuit in an RF SoC was used by DfT engineers to observe and control the receiver's channel paths. In [7], the authors proposed to characterize the eye-opening of an adaptive equalizer by observing the digital coefficients with respect to different carefully-crafted input stimuli. The authors in [8] propose algorithms for characterizing the voltage-controlled oscillator frequency by

using built-in digital self-alignment circuitry. In [9], a BIST approach built upon an all-digital phase-locked loop is demonstrated. Performance metrics, such as the phase error, can be estimated with great accuracy from the captured digital information in comparison to direct analog measurement. These reports indicate that the concept of using built-in digital calibration/adaptation units for testing analog/RF components has been applied in an ad-hoc way to specific types of circuits, but there are no systematic methods and detailed analyses for applying such methods more broadly.

In this paper, we propose a *digitally-assisted analog/RF testing* methodology for analog designs that conforms to the digitally-assisted analog/RF design styles. Instead of adding DfT circuitry to the analog domain, we modify the built-in digital structures (e.g., the digital calibration circuits) to provide observability and controllability to the internal analog paths. Test stimuli, from either the analog or digital domain, are applied to the circuit-under-test and the resulting digital data are captured for further processing to estimate the analog performance. Since we can scan in and out the internal digital data, controllability and observability to the analog/RF front-ends of the SoCs can be obtained without analog DfT. Digital data also have greater noise immunity, so the test results would be more repeatable and reliable. The proposed testing approach can be applied during the design ramp-up phase, when internal analog performance characterization is needed, and during high-volume manufacturing testing, which is useful for reducing the testing time and equipment cost.

Since the development of digitally-assisted analog circuits is design dependent, the specific DfT implementation and testing strategy for these circuits is also design dependent. In this paper, we illustrate this proposed testing approach by analyzing a digitally-calibrated Weaver image-reject receiver [10] as a case study. In [10], the calibration circuit was built-in by the designers for the purpose of performance tuning, but the possibility of re-using such a calibration circuit for production testing was not mentioned and explored. For production testing, the measurement of post-calibration specifications such as the image-rejection ratio (IRR) requires not only direct access to the analog signal path, but also lengthy testing time. In this paper, we present a method to estimate post-calibration IRR based on observing the tap coefficients. The proposed DfT modifications are non-invasive to the analog signal path and the digital test access enables repeatable and reliable measurement results. We also

discuss the Go/NoGo production testing strategies for both catastrophic and parametric faults.

The paper is organized as follows. In Section 2, we explain the motivation and concept behind digitally-assisted analog/RF design and testing. We provide a digitally-calibrated Weaver image-reject receiver case study in Section 3 and the experimental results in Section 4. We conclude the paper in Section 5.

2. Digitally-Assisted Analog/RF Design and Testing

2.1. Design Trend: Digitally-Assisted Analog/RF Design

Precision, speed, and power efficiency have been the key driving forces for analog and RF designs. *Digitally-assisted analog/RF circuits* [5] utilize the computing capability of digital circuits to achieve analog circuit performance with lower power consumption. In such a design, the digital calibration circuit enhances the analog circuit performance by setting proper values at the built-in tuning knobs. Examples designed under this principle can be found in RF front-end [10] and mixed-signal designs [11]. Digital circuits can also add flexibility to the analog circuitry that allows them to adapt to the external operating environment. Adaptive equalizer [12] is a typical example of such circuits. Moreover, high-speed digital edge transition in the nanometer regime provides finer time-domain resolution in comparison to the voltage-domain resolution in the analog domain. An all-digital phase-locked loop [13], for example, is a digitally-intensive PLL in which a time-to-digital converter is used to provide controllability and improved time-domain resolution.

The emergence of the *digitally-assisted analog design* principles' importance is evident by the dedicated special session and forum in the 2007 and 2008 International Solid-State Circuit Conferences (ISSCC). With increasingly stringent specifications in wireless communications standards and the move toward software-defined radios, incorporating digital control and calibration on chip is inevitable. Thus, for better power efficiency and greater flexibility, we expect these digitally-assisted analog design principles to be widely adopted in the future.

2.2. Digitally-Assisted Analog/RF Testing

For those analog/RF designs that follow the digitally-assisted analog/RF design guidelines, we can utilize their digital processing units to obtain controllability and observability of the internal analog paths. The conceptual diagram illustrating the digitally-assisted analog/RF design and testing is shown in Figure 1. A calibration circuit is deployed to tune the analog circuit until its performance meets a target value. In the calibration circuit, one or more analog-to-digital converters (ADCs) are used to sample the analog signals. The digital adaptation engine uses this sampled information to compute adequate digital tap coefficients for tuning the analog circuit performance. One to several digital-to-analog converters (DACs) then convert

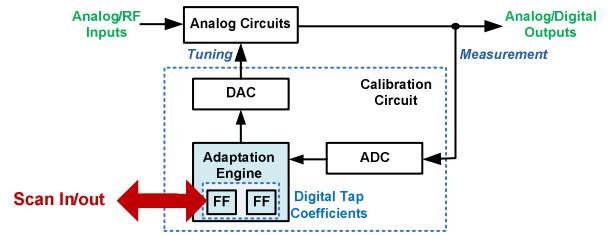


Figure 1: Conceptual Diagram of Digitally-Assisted Analog/RF Design and Testing

these digital tap coefficients into analog signals which are used to adjust the built-in tuning knobs.

This *digitally-assisted analog/RF testing* methodology, which consists of DfT modifications and testing strategy developments, can be used to support both production testing and characterization. The simplest possible DfT modification is to scan out the registers' values in the calibration circuit to assist in characterization, fault detection and diagnosis. This DfT modification is illustrated by the red arrow in Figure 1. With this DfT feature, on one hand, we can observe the analog circuit performance by scanning out digital tap coefficients during the tuning process. On the other hand, we can stress the analog circuitry by scanning specific in digital tap coefficients and observe the corresponding circuit performance at the baseband.

It is noteworthy that since the calibration circuits exist by design, clock domain disturbances and parasitics are already reduced during the design phase. Adding extra circuitry to the digital circuit will disturb the overall analog performance very little. Moreover, since the calibration circuit is reused, the proposed DfT will incur little area overhead. Compared to taking analog measurements, making measurements digitally is much cheaper and has greater noise immunity. Therefore, the test results will be much more repeatable and reliable.

3. Case Study: Testing of a Digitally-Calibrated Weaver Image-Reject Receiver

3.1. Architecture

The architecture of a digitally-calibrated Weaver image-reject receiver [10] is shown in Figure 2. This receiver utilizes a SS-LMS adaption engine, shown in Figure 3, to calibrate the intrinsic gain and phase mismatch using built-in tuning knobs. The digital portions of these devices are drawn in blue. The circuit is calibrated *offline* in the factory, with an image tone signal as the RF input. In this application, $d(t)$, the bottom input in Figure 3, is set to zero because the desired output $y(t)$ for the image tone input should be zero. The SS-LMS algorithm minimizes the difference between the signals $\varepsilon(t) = d(t) - y(t)$. During calibration, the variable gain and the variable phase blocks compensate for the intrinsic gain and phase mismatch of the original circuit based on the tap coefficients (W_1 and W_2) stored in the digital registers. W_3 is set to compensate for

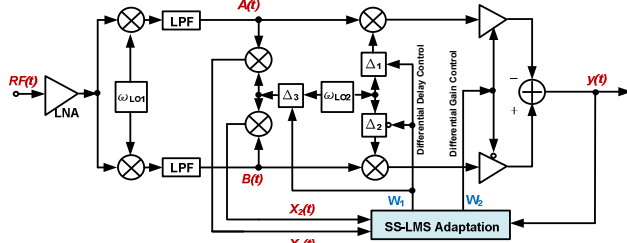


Figure 2: A digitally-calibrated image-reject receiver [10]

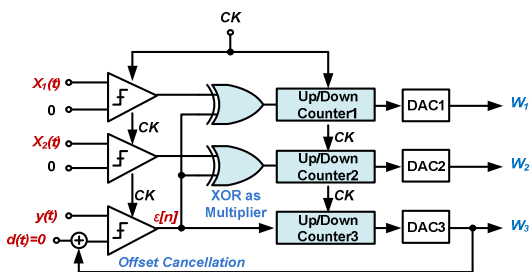


Figure 3: The SS-LMS Adaptation Engine [10]

the DC offset of the $y(t)$ comparator or the signal path because any offset will affect the convergence accuracy.

The image suppression capability of a Weaver image reject receiver depends upon the degree of gain and phase matching between the I and Q paths. The image-rejection ratio (IRR), which is the power ratio between the image signal and the desired RF signal, is a common performance metric for characterizing the efficiency of the image signal suppression. IRR can be estimated using the following equation [14]:

$$IRR(dB) = \frac{P_{im}}{P_{RF_{out}}} \approx 10 \log \frac{4}{\zeta^2 + (\Delta\theta)^2} \quad (1)$$

, where ζ is the relative gain mismatch in dB and $\Delta\theta$ is the relative phase difference in radian. Equation (1) provides a close estimation to the real IRR when the gain mismatch is relatively small compared to the signal amplitude and the phase mismatch is significantly smaller than 1 radian.

A calibrated receiver can achieve a greater IRR than an un-calibrated circuit since the received signal from the image tone is minimized to zero. The authors in [10] reported that their SS-LMS adaption engine can effectively improve the IRR from 25dB to 57dB. With this tuning capability, those design constraints mandating that I and Q must match are relaxed. Because the adaptation unit is a digital circuit, this image-reject receiver is a digitally-assisted design.

3.2. Testing considerations

IRR is an important specification for image-reject architectures that are strongly correlated to system-level specifications such as the error vector magnitude and the bit error rate. Challenges for measuring the IRR during production testing include the lack of access to internal analog signal paths, the long testing time required for high resolution measurement in the frequency domain, and the

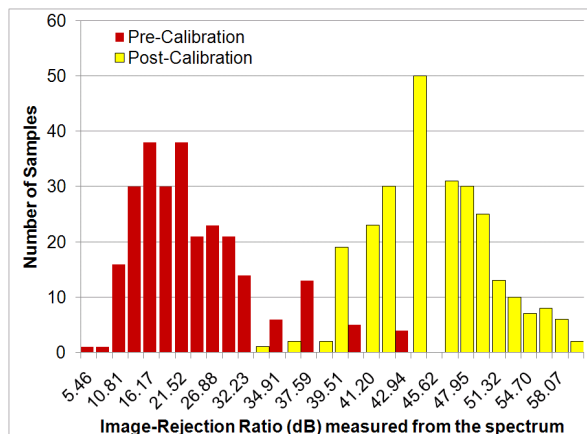


Figure 4: Image-rejection ratio histogram of 262 converged Monte Carlo simulation samples

high sensitivity to noise for the measurement. For the digitally-calibrated Weaver image reject receiver, the IRR measurement is further complicated by its calibration mechanism. On one hand, small parametric variations that distort the gain and phase mismatches can be compensated for, which effectively enhances yield. On the other hand, having a calibration mechanism does not guarantee that the post-calibration performance will meet the specifications for several reasons. The calibration circuit may itself have errors, the calibration range may not be sufficient for tuning excessive process variations, and there may exist non-ideal measurements and tuning problems in the calibration loop.

To compare the pre- and post-calibration circuit performance, we ran 300 Monte Carlo simulation samples with parametric deviations on the mathematical model of the digitally-calibrated Weaver image-reject receiver [10] using MATLAB. The gain, phase and linearity are random variables with the means set at the designed nominal values and the standard deviations set at 10%. The IRR histogram of the 262 converged samples, as shown in Figure 4, is measured from the analog output spectrum. The red bars are the pre-calibration IRR histogram, and the yellow bars show the post-calibration IRR. The chart clearly indicates that, the post-calibration IRR (ranging from 34.45 dB to 59.75 dB) is significantly greater than the pre-calibration IRR (ranging from 5.46 dB to 42.94 dB) for all the samples. This suggests that applying this calibration method, in effect, boosts the performance to a point that is near the required specifications and results in a greater chip yield.

Furthermore, any non-linearity or parametric deviations in the building blocks along the analog signal path will accumulate toward the gain/phase mismatch and be present in the IRR. Therefore, the post-calibration IRR specification will achieve better test quality for both I and Q signal paths.

Figure 4 also clearly shows that having a calibration circuit do not guarantee that a post-calibration IRR would be greater than a specified design target. After calibration, some mismatches are sufficiently compensated, but some might not be. Thus, testing for the post-calibration IRR specification remains a necessity, so does debugging for the residual mismatch.

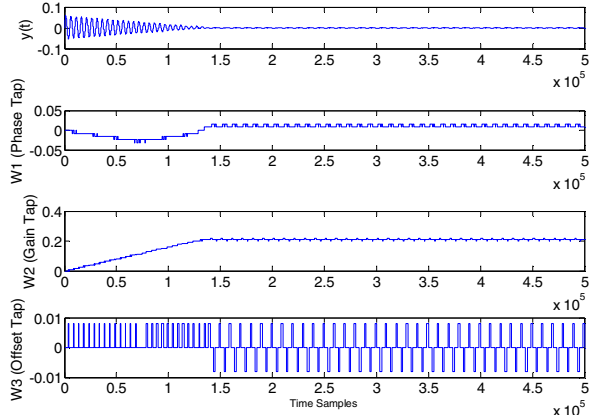


Figure 5: Waveforms illustrating the tuning

3.3. Using Calibration Circuits for IRR Estimation

Conceptually, a calibration procedure consists of two steps: measuring circuit performance and adjusting performance to meet a specific target by changing the built-in tuning knobs. The SS-LMS adaptation engine in particular, calibrates a circuit through continuously alternating between measurement and adjustment. The algorithm converges when the difference between the sensed value and the target performance value is minimized. It is noteworthy that, when equilibrium is reached, i.e., the adaption engine converges, the tap coefficients still continuously toggle for at least one least significant bit (LSB). This is because the adaption engine constantly introduces one LSB of gain and phase mismatch as part of the tuning process. After the target performance level is achieved, adding additional mismatch will lead to over compensation and results in mismatch in another direction. In the following cycle, the adaption engine will compensate for the newly induced mismatch by reversing the process. Therefore, the tap coefficients from the adaptive engine will not maintain a constant value even when the values converge.

To prevent excessive oscillation resulting from noise, some form of masking can be deployed. With masking, the tap coefficients increase or decrease by a fixed step only after several consecutive commands which request change in the same direction are received. In the circuit implementation [10], the up/down counters are 14-bits wide, but the DACs have only 11-bit resolution, thus providing a 3-bit masking. In other words, the output of the DAC will increase or decrease after eight consecutive increase or decrease commands are received.

To illustrate, the result of the tuning procedure applied to one design instance is shown in Figure 5. The top curve represents $y(t)$ and the bottom three curves represent the W_1 , W_2 , and W_3 tap coefficients for gain, phase and offset compensation. During the tuning process, the $y(t)$ amplitude is gradually suppressed until it matches the desired zero $d(t)$. The tap coefficients converge after approximately 2×10^5 time samples. After convergence, a steady-state variance can be observed. The adaption engine runs at 10 MHz while the rest

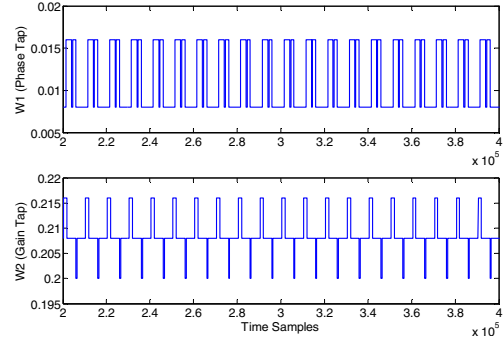


Figure 6: The convergence region of coefficients W_1 and W_2 given in Figure 5 shown in detail

of the system runs at 5 GHz per sample. The tap coefficients in this simulation example required about 40 μ sec to converge, while a silicon prototype reported in [10] took about 4 msec.

To estimate the post-calibration IRR performance, we need to know the *residual gain and phase mismatch* which are not compensated by the calibration. These mismatches can result from quantization errors, limited tuning resolution, nonlinearity of the tuning circuitry, or offsets in the comparators. Let \hat{w}_1 and \hat{w}_2 be the residual gain and phase mismatch after convergence, we can estimate the post-calibration IRR using a similar equation as equation (1):

$$IRR(dB)|_{\text{post-calibration}} \approx 10 \log \frac{4}{\hat{w}_1^2 + \hat{w}_2^2} \quad (2)$$

Note that \hat{w}_1 and \hat{w}_2 are the normalized phase and gain tap coefficient values. \hat{w}_1 is normalized to 1 radian phase mismatch compensation per unit of W_1 and \hat{w}_2 is normalized to 1 dB of gain mismatch compensation per unit of W_2 . A first order estimation of these residual mismatches is the steady state variance of the tap coefficient. After convergence (i.e. the calibration process is completed), the steady state variance can be defined as the difference between the maximum and minimum values of the tap coefficient.

As an example, detail of the converged regions of coefficients W_1 and W_2 shown in Figure 5 are shown in Figure 6. In this figure, the value of \hat{w}_1 is 0.008 and \hat{w}_2 is 0.016. Using Equation (2), the estimated post-calibration performance is 40.969 dB, compared to the measurement taken from the analog spectrum, which is an IRR of 42.23 dB.

3.4 Proposed DfT Modifications

The required DfT for accessing the tap coefficients is to connect the three up/down counters to a scan chain, as shown in green in Figure 7. Such a scan chain can be inserted using a commercially available synthesis tool and does not require extra I/O pins since these scan signals will be connected through JTAG, which is shared in an SoC. Therefore, the overall overhead for this DfT modification is low. The DfT modifications are completely in the digital domain and are non-invasive to the analog signal path and, thus, they will not affect the analog performance.

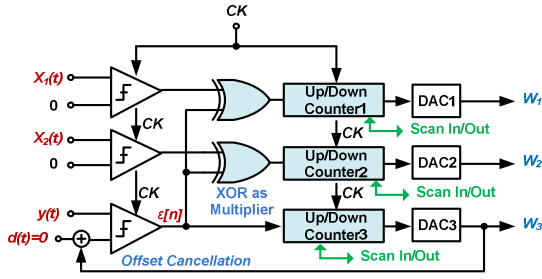


Figure 7: Proposed DFT modifications

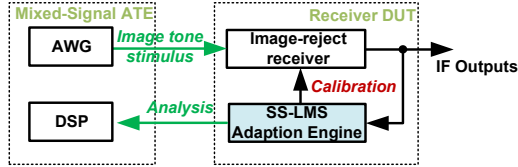


Figure 8: Calibration and production testing setup

3.5. Digitally-Assisted Production Testing Strategy

With a built-in calibration engine, we can perform Go/No-Go testing based on the observed tap coefficients in the following scenarios. Since each circuit has a limited built-in tuning range, saturation in any of the tap coefficients (W_1 , W_2 , or W_3) is an indication of excessive and un-compensatable deviations. Furthermore, since the coefficients produced by the SS-LMS engine will converge with a small steady-state variance, receivers with constant or unsettled coefficients from the SS-LMS adaptation engine would indicate excessive process variations, non-monotonicity, or a catastrophic error. All these scenarios imply that the adaption engine fails to calibrate the circuit and the resulting IRR will very likely fail the specifications. Therefore, such instances should be screened out.

If the tap coefficients do converge with a small steady-state variance, the post-calibration IRR can be estimated using Equation (2) and a Go/NoGo decision can be made based on the IRR specification requirement.

The calibration and testing setup is shown in Figure 8. Here, the arbitrary waveform generator (AWG) produces an image tone and the DSP captures values in the three up/down counters for analysis. This test is very repeatable and robust because the digital domain has greater noise immunity.

As discussed in Section 3.2, the circuit will be shipped in a post-calibration mode and, thus, all chips must be calibrated before production testing. With the proposed approach, production testing and calibration could actually be merged into a single process – the tap coefficients are monitored during calibration and the observed results are also used for the screening decision. Therefore, IRR testing will not incur any additional time beyond calibration. The conceptual diagram showing the testing time reduction of our proposed test strategy is illustrated in Figure 9. Defective parts that fail the IRR specifications can be screened out early to reduce the overall testing cost.

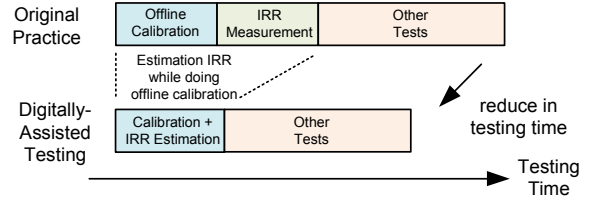


Figure 9: Conceptual diagram of test time reduction using digitally-assisted testing approach

4. Experimental Result

To validate our proposed approach, we built a MATLAB simulation model of a digitally-calibrated Weaver image-reject receiver. The design parameters of the building blocks – such as the gain and the IIP3 for the LNA and the mixers, the insertion loss and delay for filters, the unit gain of tuning circuits, and the offset of the comparators – are considered random variables of a normal distribution with the means at their nominal values and a standard deviation of 10%. We then generate a large number of instances for simulation.

To evaluate the detectability for catastrophic faults, we injected stuck-at-zero and stuck-at-one faults at the wires shown in Figures 2 and 3. The digital tap coefficients of all faulty circuits have one of the following phenomena: 1) one or more coefficients remain constant; or 2) the coefficients fail-to-converge or saturate. The experimental results also indicated that all the stuck-at faults in the digital calibration circuits can be detected.

For the following experiments, we ran 300 Monte Carlo simulation instances. For each instance, we assume the design parameters are random variables with the means at their nominal values and a standard deviation of 10%. After adaption, the tap coefficients of 1 instance saturate, 37 instances diverge and the rest converge. Here, divergence means that the tap coefficients do not converge to a value within the designated calibration time. This may result from slow-to- or never-converge behaviors and such a chip should be marked as failed. In calibration and production testing, limited time will be given to evaluate each chip. The one instance which saturates has excessive parametric faults variation beyond calibratable range.

For converged instances, we can estimate the IRR performance to determine whether the specification is met. For post-calibration IRR estimation, we first obtain the steady-state variances of the tap coefficients after convergence. Note that the steady-state variances are captured from the up-down counters before 3-bit masking is applied. In other words, the observed steady-state variances are different from the steady-state variances of the actual tuning signal: the former is from the 14-bit counters and the latter is from the 11-bit DACs.

In our experiment, the steady-state variance is calculated by subtracting the maximum coefficient value from the minimum after the tap coefficient converges. This number is then rounded to the closest multiple of the calibration resolution. Specifically, in our simulation, the

phase (W_1) and gain (W_2) coefficients are set to compensate for 0.00042 radian and 0.0017 dB of phase and gain mismatch per 3-bit LSB [10], taking into account the 3-bit masking. For example, if the obtained gain coefficient oscillation range is 0.02975, it would be rounded to 0.0289, which is the closest multiple of 0.0017.

The estimated and measured post-calibration IRR results are shown in Figure 10. The horizontal axis is the measured IRR from the analog spectrum and the vertical axis is the estimated IRR based on Equation (2). Each point represents a simulation instance, and a point that is located on the diagonal line implies perfect matching between the estimated and the measured values. The results show that the IRR estimation is somewhat pessimistic as most of the instances fall toward the right of the diagonal line. The absolute value of the post-calibration estimation error has a mean of 9.13%, and a standard deviation of 7.43%.

The discrepancy between the estimated IRR and the actual measurement is partially caused by the quantization error in the adaptation engine. Specifically, the finite compensation resolution introduces a quantization error because the gain and phase compensation is discrete and the exact amount of mismatch may not be found. Although 3-bit masking reduces the amount of tap coefficient oscillation, it introduces a larger quantization error since any gain/phase mismatch that is sensed will not be immediately compensated for until the mismatch exceeds the masking level. The noise and offsets of the $y(t)$ comparator also contribute additional errors to the measurement result and reduce the accuracy of the IRR estimation. Moreover, due to process variations, the amount of gain or phase mismatch induced by changing one bit of the tap coefficient may deviate from the nominal values. Finally, Equation (2) is an approximation of the circuit IRR and is more accurate when the gain and phase mismatch are relatively small compared to the nominal design values.

5. Conclusion

We propose a digitally-assisted analog/RF testing methodology for characterizing and testing digitally-assisted analog designs. We use a digitally-calibrated Weaver image-reject receiver to illustrate the proposed test strategies and to demonstrate the method of reusing the built-in calibration circuitry for close analog performance estimation. By adding a scan structure to the digital calibration circuitry, the analog circuitry can be characterized without direct access to any analog signals.

This testing methodology should be applicable to a wide range of analog and RF systems and is especially suitable for characterizing and testing the analog/RF frontend in a mixed-signal SoC. The DfT modifications are noninvasive to the analog path and can be easily extended for BIST implementation. With this testing method, digitally-assisted analog circuits can not only be calibrated for performance enhancement, but also can be tested at a low cost.

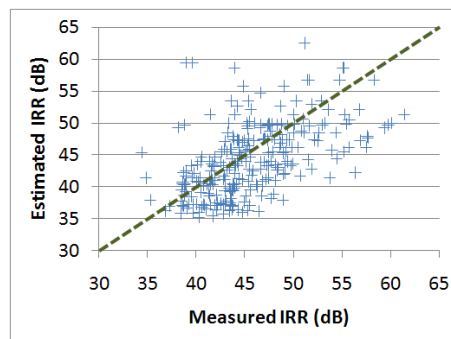


Figure 10: Estimated and measured post-calibration Image-Rejection Ratio (IRR)

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References

- [1] J. Ferrario, R. Wolf, S. Moss, and M. Slamani, "A Low-Cost Test Solution for Wireless Phone RFICs," *IEEE Communication Magazine*, Sept. 2003.
- [2] Karim Arabi and Bozena Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 7, July 1997.
- [3] Linda S. Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, vol.45, no. 10, Oct. 1998.
- [4] A. Valdes-Garcia, J. Silva-Martinez, and E. Sanchez-Sinencio, "On-Chip Testing Techniques for RF Wireless Transceivers," *IEEE Design and Test of Computers*, July-Aug. 2006.
- [5] B. Murmann, "Digitally-assisted analog circuits," *IEEE Micro*, vol. 26, no. 2, pp.38-47, Mar.-Apr. 2006.
- [6] S. Abdennadher and S. A. Shaikh, "Practices in Mixed-Signal and RF IC Testing," *IEEE Design and Test of Computers*, July-Aug. 2007.
- [7] M. Lin and K.-T. Cheng, "Testable Design for Adaptive Linear Equalizer in High-Speed Serial Links," in *Proc. of IEEE International Test Conference (ITC)*, Oct. 2006.
- [8] F. Demmerle, "Integrated RF-CMOS Transceivers Challenge RF Test," in *Proc. of IEEE International Test Conference (ITC)*, Oct. 2006.
- [9] R. B. Staszewski, I. Bashir, and O. Eliezer, "RF Built-in Self Test of a Wireless Transmitter," *IEEE Trans. on Circuits and Systems II. - Express Briefs*, vol. 54, no. 2, pp. 186-190, Feb. 2007.
- [10] L. Der and B. Razavi, "A 2-GHz CMOS Image-Reject Receiver with LMS Calibration," *IEEE J. of Solid-State Circuits*, vol. 38, no. 2, pp. 167-175, Feb. 2003.
- [11] R. H.M. van Veldhoven, R. Rutton, and L. J. Breems, "An Inverter-Based Hybrid $\Sigma\Delta$ Modulator," in *Proc. of IEEE International Solid State Circuits Conference (ISSCC)*, Feb. 2008.
- [12] V. Stojanovic, A. Ho, B.W. Garlepp, F. Chen, J. Wei, G. Tsang, E. Alon, R. T. Kollipara, C.W. Werner, J. L. Zerbe, M. A. Horowitz, "Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," *IEEE J. of Solid-State Circuits*, vol. 40, no. 4, pp. 1012-1026, Apr. 2005.
- [13] R. B. Staszewski, J. Wallberg, S. Rezeq et al, "All-digital PLL and transmitter for mobile phones," *IEEE J. of Solid-State Circuits*, vol. 40, no. 12, pp. 2469-2482, Dec. 2005..
- [14] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2003.